What is claimed is:

CLAIMS

1. A method of assembling devices comprising:

providing a temporary carrier substrate with first and second surfaces, the first surface is prepared with an adhesive;

mating a structural member on the carrier substrate, the structural member comprising a plurality of die package regions, wherein a package region comprises a die attach region surrounded by a peripheral region; and

attaching dies in the die attach regions of the structural member,

wherein through-vias are disposed in the package regions of the structural member, the through-vias comprise a conductive material, the through-vias are electrically coupled to bond pads of the dies.

2. The method of claim 1 wherein:

the die attach regions comprise openings extending through surfaces of the structural member; and

attaching dies include disposing dies in the openings for temporary attachment to the carrier substrate.

3. The method of claim 2 comprises:

encapsulating the dies with a mold compound;

curing the mold compound, wherein the structural member reduces warpage;

removing the temporary support carrier; and

separating the structural member to form individual packages.

4. The method of claim 3 wherein:

a thickness of the structural member is about equal to a thickness of the die to produce top surfaces of the mold compound, die and structural member which are about coplanar; or

a thickness of the structural member is greater than a thickness of the die to produce top surfaces of the mold compound and structural member which are about coplanar.

5. The method of claim 4 comprises:

forming a top RDL layer on top surfaces of the encapsulated dies; and

forming a bottom RDL layer on bottom surfaces of the encapsulated dies after removing the temporary support carrier, wherein the RDL layers and through vias facilitate stacking of packages.

6. The method of claim 3 wherein a thickness of the structural member is less than a thickness of the die.

7. The method of claim 6 comprises:

forming a top RDL layer on top surfaces of the encapsulated dies; and

forming a bottom RDL layer on bottom surfaces of the encapsulated dies after removing the temporary support carrier, wherein the RDL layers and through vias facilitate stacking of packages.

8. The method of claim 2 wherein through-vias are disposed in the peripheral regions of the package regions.

9. The method of claim 8 comprises:

encapsulating the dies with a mold compound;

curing the mold compound, wherein the structural member reduces warpage;

removing the temporary support carrier; and

separating the structural member to form individual packages.

10. The method of claim 9 wherein:

a thickness of the structural member is about equal to a thickness of the die to produce top surfaces of the mold compound, die and structural member which are about coplanar; or

a thickness of the structural member is greater than a thickness of the die to produce top surfaces of the mold compound and structural member which are about coplanar.

11. The method of claim 10 comprises:

forming a top RDL layer on top surfaces of the encapsulated dies; and

forming a bottom RDL layer on bottom surfaces of the encapsulated dies after removing the temporary support carrier, wherein the RDL layers and through vias facilitate stacking of packages.

12. The method of claim 1 wherein the structural member comprises a planar surface in which package regions are defined.

13. The method of claim 12 wherein the dies comprises flip chips.

14. The method of claim 12 wherein the structural member serves as an interposer between a die and a substrate of a package.

15. The method of claim 12 wherein the structural member comprises through-vias distributed in the package regions.

16. The method of any one of claims 1-15 wherein the structural member comprises a material for balancing coefficient of thermal expansion (CTE).

17. The method of any one of claims 1-15 wherein the structural member facilitates assembling devices in a wafer format.

18. A semiconductor package comprising:

a structural member having first and second major surfaces, the structural member includes

a die attach region defined in the structural member, the die attach region accommodates a die for packaging,

a peripheral region surrounding the die attach region, and

at least one through-via disposed in the structural member, the through-via extending through the first and second surfaces of the structural member.

19. The semiconductor package of claim 18 wherein:

the structural member comprises an opening through the major surfaces;

the die is disposed in the opening; and

through-vias are disposed in the peripheral region.

20. The semiconductor package of claim 18 wherein:

the die is attached to the first major surface of the structural member in the die attach region;

the through-vias are disposed in the structural member in the die attach region; and

the structural member serves as an interposer between the die and a substrate.

21. A method of assembling a device comprising:

providing a temporary carrier substrate with first and second surfaces, the first surface is prepared with an adhesive;

mating a structural member on the carrier substrate, the structural member comprising a die package region, wherein the package region comprises a die attach region surrounded by a peripheral region; and

attaching a die in the die attach region of the structural member, wherein at least one through-via is disposed in the structural member,

wherein through-vias are disposed in the package region of the structural member, the through-vias comprise a conductive material, the through-vias are electrically coupled to bond pads of the die.

What is claimed is:

CLAIMS

1. A semiconductor package comprising:

a structural member having first and second major surfaces, the structural member includes

a die attach region defined in the structural member, the die attach region accommodates a die for packaging and includes an opening passing through the major surfaces,

a peripheral region surrounding the die attach region,

at least one through-via disposed in the structural member, the through-via extending through the first and second surfaces of the structural member; and

a die being disposed in the opening, the die is smaller than the opening and gaps exist between the die and sidewalls of the opening, and the gaps are filled with a mold compound to encapsulate the die,

wherein a thickness of the structural member is less than a thickness of the die.

2. The semiconductor package of claim 1 comprises:

a top RDL layer on a top surface of the encapsulated die; and

a bottom RDL layer on a bottom surface of the encapsulated die, wherein the RDL layers and the at least one through-via facilitates stacking of packages.

3. The semiconductor package of claim 1 wherein the mold compound covers the first major surface of the structural member.

4. The semiconductor package of claim 3 wherein the at least one through-via extends through the mold compound and the first and second major surfaces of the structural member.

5. The semiconductor package of claim 4 wherein the structural member and the mold compound are separate components and comprise the same material.

6. The semiconductor package of claim 5 wherein the die includes first and second die surfaces, wherein the first die surface is an active surface and the first die surface is coplanar with a first surface of the mold compound.

7. The semiconductor package of claim 1 wherein the structural member and the mold compound are separate components and comprise the same material.

8. The semiconductor package of claim 6 wherein the second die surface is an inactive surface and the second die surface is coplanar with a second surface of the mold compound and the inactive surface of the die is exposed.

9. The semiconductor package of claim 1 wherein the mold compound covers the first major surface of the structural member and the die.

10. The semiconductor package of claim 1 wherein the structural member facilitates assembling devices in a wafer format.

11. The semiconductor package of claim 10 wherein the structural member and the mold compound are separate components and comprise the same material.

12. The semiconductor package of claim 11 wherein the mold compound covers the first major surface of the structural member.

13. The semiconductor package of claim 12 wherein the at least one through-via extends through the mold compound and the first and second major surfaces of the structural member.

14. The semiconductor package of claim 13 comprises:

a top RDL layer on a top surface of the encapsulated die; and

a bottom RDL layer on a bottom surface of the encapsulated die, wherein the RDL layers and the at least one through-via facilitates stacking of packages.

15. The semiconductor package of claim 13 wherein the die includes first and second die surfaces, wherein the first die surface is an active surface and the first die surface is coplanar with a first surface of the mold compound.

16. The semiconductor package of claim 15 wherein the second die surface is an inactive surface and the second die surface is coplanar with a second surface of the mold compound and the inactive surface of the die is exposed.

17. The semiconductor package of claim 9 wherein the structural member and the mold compound are separate components and comprise the same material.

18. The semiconductor package of claim 17 wherein the at least one through-via extends through the mold compound and the first and second major surfaces of the structural member.

19. The semiconductor package of claim 17 wherein the die includes first and second die surfaces, wherein the first die surface is an active surface and the first die surface is coplanar with a first surface of the mold compound.

20. The semiconductor package of claim 19 comprises:

a top RDL layer on a top surface of the encapsulated die; and

a bottom RDL layer on a bottom surface of the encapsulated die, wherein the RDL layers and the at least one through-via facilitates stacking of packages.