

CELL STRUCTURE FOR DUAL-PORT SRAM

ABSTRACT

The present disclosure provides a dual port static random access memory (SRAM) cell. The dual-port SRAM cell includes a first and second inverters cross-coupled for data storage, each inverter includes a pull-up device (PU) and a plurality of pull-down devices (PDs); a plurality of pass gate devices configured with the two cross-coupled inverters; and at least two ports coupled with the plurality of pass gate devices (PGs) for reading and writing, wherein each of PU, PDs and PGs includes a fin field-effect transistor (FinFET), a ratio between a number of PDs in the SRAM cell and a number of PGs in the SRAM cell is greater than 1, and a number of FinFETs in the SRAM cell is equal to or greater than 12.

Figure 1