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Process for forming a housing for electronic modules, and
electronic modules hermetically encapsulated in this way

5 Description

The invention relates to a process for forming housings for electronic modules, and to electronic modules that are hermetically encapsulated in this way, in particular sensors,
10 integrated circuits and optoelectronic components.

To encapsulate integrated circuits and optoelectronic components, it is known to use an organic adhesive layer to bond a thin plate of glass onto the module and thereby to
15 cover and protect the sensitive semiconductor structures. This design has the drawback that over the course of time water can diffuse into the organic adhesive layer and can then reach and damage the semiconductor structures. Furthermore, the adhesive layers may age as a result of UV
20 irradiation, which is damaging in particular to electro-optical modules.

As an alternative to organic adhesives, low-melting glass solder has also already been used as an intermediate layer
25 which has been sprayed on, sputtered on or applied by means of screen-printing and dispenser technology. The process temperature for melting the glass-solder layer, however, is higher than $T=300^{\circ}\text{C}$, which means that temperature-sensitive semiconductor structures cannot be encapsulated.

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The invention is therefore based on the object of providing a

process for encapsulating electronic modules which makes it possible to achieve encapsulation which is substantially resistant to water diffusion yet is carried out at moderate temperatures below 300°C, preferably below 150°C.

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The object set is achieved on the basis of the measures described in claim 1 and is configured and developed further by the further measures of the dependent claims. Claim 24 relates to an electronic module producible in accordance with the invention, with advantageous refinements and configurations being given in the claims that are dependent on claim 24.

One advantage of coating with a vapor-deposition glass is the application of the insulating glass layer at room temperature up to approximately 150°C, so that there is no likelihood of damage or oxidation of the substrate surface whatsoever, even with metal substrates. In this context, reference is also made to the following applications:

20 DE 202 05 830.1, filed on 04.15.2002,
DE 102 22 964.3, filed on 05.23.2002;
DE 102 22 609.1, filed on 05.23.2002;
DE 102 22 958.9, filed on 05.23.2002;
DE 102 52 787.3, filed on 11.13.2002;
25 DE 103 01 559.0, filed on 01.16.2003;
in the name of the same Applicant, the content of disclosure of which is hereby expressly incorporated by reference.

With regard to the barrier properties of vapor-deposition glass layers, measurements have shown that with layer thicknesses of the vapor-deposition glass layer in the range from 8 µm to 18 µm, helium leak rates of less than 10⁻⁷ mbar l s⁻¹ or less than 10⁻⁸ mbar l s⁻¹ are reliably achieved. The measurements, for layers with a thickness of 8 µm and 18 µm

have even revealed helium leak rates of between 0 and 2×10^{-9} mbar l s⁻¹, and even these upper limit values are significantly influenced by the measurement inaccuracy of the tests carried out.

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The process according to the invention for encapsulation with vapor-deposition glass can even be employed if the electronic module is attacked while it is still being produced.

10 The thickening of the substrate of the electronic module produced by the vapor-deposited glass layer is utilized to stabilize the substrate while actions are being carried out on the substrate from the unencapsulated side. The otherwise finished electronic module may also be encapsulated from the connection side, leaving clear the connections themselves.
15 For this purpose, the substrate may, for example, be provided with a passivation layer on the opposite side from a first side having the semiconductor structures. By way of example, a plastic layer is suitable for this purpose. The passivation
20 layer may also comprise a glass layer which is preferably vapor-deposited onto this side.

The process is particularly suitable for packaging components which still form part of a wafer (wafer level packaging), in
25 which case the substrate comprises a wafer having the substrates of the components, which can be separated from the wafer after they have been packaged.

Depending on the particular requirements, the thickness of
30 the vapor-deposited glass layer may be from 0.01 to 1000 μm . If it is merely a matter of hermetically sealing the module to be protected, it is preferable for the glass layer thickness to be in the range between 0.1 and 50 μm . If the loads imposed are greater, the glass layer thickness is

increased accordingly, with a preferred range for the glass layer thickness being between 50 and 200 μm . It is also possible to build up multiple layers in combination with other materials. It is, furthermore, possible for the glass
5 layer to be combined with an applied plastic layer in order to structurally reinforce the electronic module.

There are various options for the vapor deposition of glass. It is preferable to generate the glass vapor from a stock
10 glass target by means of electron beam. It is possible to generate vapor-deposition rates of more than 4 $\mu\text{m}/\text{min}$, and the glass produced is deposited with a secure bond on the surface of the substrate without needing an increased H_2O content for a bonding action, as is the case with low-melting
15 glass solder. The preferred vapor-deposition glass is a borosilicate glass containing aluminum oxide and alkali metal oxide fractions, such as for example the vapor-deposition glass of type 8329 produced by Schott Glas. Moreover, this glass has a coefficient of thermal expansion which is close
20 to that of the substrate for standard semiconductor structures or can be matched to the coefficient of thermal expansion of the substrate by suitable modification to the components. It is possible to use vapor-deposition glass of other compositions, in particular in a plurality of layers on
25 top of one another, in which case the glasses of the layers may have different properties with regard to refractive index, density, hardness, etc.

The vapor-coating of the substrate with a glass layer may
30 advantageously also encompass plasma ion assisted deposition (PIAD). In this case, an ion beam is additionally directed onto the substrate to be coated. The ion beam may be produced by way of a plasma source, for example by ionization of a suitable gas. The plasma results in additional densification

of the layer and the removal of loosely adhering particles from the substrate surface. This leads to particularly dense, low-defect deposited layers.

5 Furthermore, by selecting a suitable combination of materials, it is possible to realize the application of a mixed layer of inorganic and organic constituents. This mixed layer is characterized by a reduction in its brittleness.

10 If the glass layer is applied to a first side of the substrate of the electronic module before this electronic module has been fully produced, it may be expedient, for handling purposes during completion of production, to apply a plastic layer, which reinforces the module, above the glass
15 layer. In this case, the glass layer is produced with a thickness which is sufficient for encapsulation or hermetic seal with respect to the penetration of diffusing substances, while the plastic layer is produced in a thickness which is required for stabilization during further processing of the
20 module.

In such a case, it is possible for material to be removed from the second, unencapsulated substrate side, so that it is possible to produce connections to the module which extend
25 into the module from the underside and are therefore protected by the module itself when the module is finally installed at its position of use. This is of significance in particular in the case of sensors.

30 The invention is described with reference to the drawing, in which:

Fig. 1 shows a section through a wafer with a vapor-deposited glass layer,

- Fig. 2 shows a wafer section with glass and plastic layer,
- Fig. 3 shows the production of connections to the wafer,
- 5 Fig. 4 shows the additional plastic passivation of the wafer underside,
- Fig. 5 shows the coating of the wafer underside with vapor-deposition glass,
- Fig. 6 shows the application of a ball grid array to the wafer shown in Fig. 5,
- 10 Fig. 7 shows a further way of applying the ball grid array,
- Fig. 8 shows the encapsulation of the underside of a wafer,
- 15 Fig. 9 shows the application of the ball grid arrays to the wafer shown in Fig. 8,
- Fig. 10 shows a diagram illustrating a vaporization arrangement,
- Fig. 11 shows results of a TOF-SIMS measurement, and
- 20 Fig. 12 shows an electron microscope transverse microsection image.

Fig. 10 shows the arrangement of a substrate 1 with respect to a vapor-deposition glass source 20 which comprises an

25 electron beam generator 21, a beam-diverter device 22 and a glass target 23 on which the electron beam 24 impinges. At the location at which the electron beam impinges, the glass is vaporized and is then deposited on the first side 1a of the substrate 1. To allow the glass from the target 23 to be

30 vaporized as uniformly as possible, the target is rotated and the beam 24 sweeps back and forth along it. In addition, the arrangement may also comprise a plasma source for generating an ion beam which, in operation, is directed onto the side 1a that is to be coated, in order for the substrate to be coated

35 with a glass layer by means of plasma ion assisted deposition

(PIAD) .

For more details concerning the possible substrate 1, reference is made to Fig. 1. A silicon wafer as the substrate 1 includes regions 2 having semiconductor structures and regions 3 having connection structures, for example made from aluminum. The connection structures may, for example, comprise bond pads or other connection surfaces. The silicon wafer constitutes a substrate with a surface roughness of < 5 μm . The top side 1a of the substrate is on the opposite side from the underside 1b. A glass layer 4, which has preferably been obtained from the vapor-deposition glass of type 8329 produced by Schott, has been deposited on the top side 1a. This type of glass can be substantially vaporized by the action of the electron beam 24, the work being carried out in an evacuated environment at 10^{-4} mbar residual pressure and a bias temperature during the vaporization of 100°C. Under these conditions, a dense, continuous glass layer 4 is produced, and this layer is substantially impermeable to gases and liquids, including water, but transmits light, which is important in the case of electro-optical modules.

The glass layer 4 may also include a plurality of individual layers, for example made from glasses with different compositions. The glass layer may also comprise a mixed layer formed from inorganic and organic constituents in order, for example, to achieve an increased layer flexibility.

The underside 1b of the wafer is available for further processing steps, which include wet, dry and plasma etching or cleaning.

If, as in Fig. 1 and the further Figs. 2 to 9, the substrate used is a wafer, the process according to the invention may

expediently be used to package components which still form part of a wafer. However, the process can also be applied in a similar way to chips which have already been separated from the wafer and comprise semiconductor structures and connection structures.

Fig. 2 shows a covering layer for the substrate 1, comprising a glass layer 4 and a plastic layer 5. The glass layer 4 has a thickness in the range from 1 to 50 μm , which is sufficient for the encapsulation or hermetic sealing, while the plastic layer 5 is thicker, in order to impart greater stability to the wafer as a workpiece for subsequent treatment steps.

Fig. 3 shows the further treatment of a wafer. The wafer is thinned on the underside, so that the components that can be produced in accordance with the invention have a thinned substrate, and etching pits 6 are produced, extending as far as the connection structures 3, which act as an etching stop. The wafer underside 1b is provided with a plastic lithograph, with the regions of the connection structures 3 remaining open. Then, line contacts 7 are produced on the underside, for example by spraying or sputtering, with the result that conductive layers 7 are produced in the region of the etching pits 6. Then, the plastic used for the lithography is removed from the wafer underside 1b. Next, a ball grid array 8 is applied to the conductive layers 7, and the wafer is divided along planes 9. The result is a plurality of electronic modules whose semiconductor structures 2 are safely embedded between the covering layer 4 and the substrate 1 such that they are hermetically sealed.

Fig. 4 shows a modification to the embodiment shown in Fig. 3. The same process steps as those described above are carried out, but the plastic on the wafer underside 1b is not removed and covers the underside as a passivation and

protective layer 10.

Fig. 5 shows an embodiment in which a vapor-deposited glass layer 11 is to be applied to the underside 1b of the substrate instead of the plastic layer 10. As in the
5 embodiment shown in Fig. 3, the plastic used for lithography is removed from the wafer underside 1b, and the entire underside 1b of the wafer is vapor-coated with the glass, producing a 1 to 50 μm thick glass layer 11.

10 The glass layer 11 shown in Fig. 5, like the plastic layer 10 illustrated in Fig. 4, serves as a protective or passivation layer.

15 As illustrated at 11b, this glass layer also covers the outwardly projecting parts of the line contacts 7. To apply a ball grid array 8, these regions 11b are uncovered by being ground and/or etched away. Then, the ball grid arrays are applied, as shown in Fig. 6, and the wafer is then divided up
20 in order to form individual modules, and indicated at 9. The sensitive semiconductor structures 2 are protected at the top and the bottom by a respective glass layer 4 and 11.

In a further embodiment of the invention, the wafer is
25 divided up at parting planes 9 which do not pass through the connection structures. This has the advantage that it is also possible to ensure a lateral passivation protection for the modules. Fig. 7 shows an example of dividing up the wafer which only affects material of the covering layer 4 and of
30 the substrate 1. The procedure is initially the same as for the exemplary embodiments described above, i.e. the wafer is thinned from the underside and etching pits 6 which extend as far as the underside of the connection structures 3 are produced. The wafer underside 1b is lithographed, with the
35 regions of the connection structures remaining open. The line

contacts 7 are produced in the region of the etching pits 6, with the etching pits also being filled with conductive material 12. In this context, thickening by electroplating using Ni(P) may be considered. The components producible in accordance with this embodiment of the invention accordingly have through-contacts passing through the substrate.

After the plastic has been removed from the wafer underside at least in the region of the contacts 7, the ball grid arrays 8 are applied. This is followed by dividing up the wafer along planes 9. The result is electronic modules with hermetically sealed semiconductor structures 2, with an analogous plastic layer 10 being present or absent depending on the procedure employed.

Figs. 8 and 9 show an exemplary embodiment involving the production of a glass layer 11 on the underside. The procedure is similar to that of the embodiment shown in Fig. 5 in conjunction with Fig. 7, i.e. filled regions are produced beneath the connection structures, and the entire underside 1b of the wafer is coated with the glass layer 11, which is then removed in the region of the filled etching pits 6 in order for the ball grid arrays to be applied thereto, as shown in Fig. 9. After the wafer has been divided up along planes 9, modules with encapsulated semiconductor structures 2 are obtained.

The glass system of the layer 4 or 11 should form at least a binary system. Multicomponent systems are preferred.

Vapor-deposition glass which has the following composition, in percent by weight, has proven particularly suitable:

Components	% by weight
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	SiO ₂	75 - 85
	B ₂ O ₃	10 - 15
	Na ₂ O	1 - 5
	Li ₂ O	0.1 - 1
5	K ₂ O	0.1 - 1
	Al ₂ O ₃	1 - 5

A preferred vapor-deposition glass of this type is glass 8329 produced by Schott, having the following composition:

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SiO ₂	84.1%
B ₂ O ₃	11.0%

	Na ₂ O	≈	2.0%]
15	K ₂ O	≈	0.3%} 2.3% (in the layer ? 3.3%)
	Li ₂ O	≈	0.3%]
	Al ₂ O ₃	≈	2.6% (in the layer < 0.5%)

20 The values given in parentheses represent the proportions by weight of the respective component in the vapor-deposited layer.

25 The electrical resistance is approximately 10^{10} Ω/cm (at 100°C),
the refractive index is approximately 1.470,
the dielectric constant ϵ is approximately 4.7 (at 25°C, 1 MHz), and $\text{tg}\delta$ is approximately 45×10^{-4} (at 25°C, 1 MHz).

30 A further group of suitable vapor-deposition glasses has the following composition, in percent by weight:

Components: % by weight

	SiO ₂	65 - 75
	B ₂ O ₃	20 - 30
	Na ₂ O	0.1 - 1
	Li ₂ O	0.1 - 1
5	K ₂ O	0.5 - 5
	Al ₂ O ₃	0.5 - 5

A preferred vapor-deposition glass from this group is the glass G018-189 produced by Schott having the following composition:

	Components:	% by weight
	SiO ₂	71
	B ₂ O ₃	26
15	Na ₂ O	0.5
	Li ₂ O	0.5
	K ₂ O	1.0
	Al ₂ O ₃	1.0

The glasses 8329 and G018-189 that are preferably used in particular have the properties as listed in the table below:

Properties	8329	G018-189
$\alpha_{20-300} [10^{-6} K^{-1}]$	2.75	3.2
Density (g/cm ³)	2.201	2.12
Transformation point [°C]	562	742
Refractive index n_d	1.469	1.465
Hydrolytic resistance class according to ISO 719	1	2
Acid resistance class according to DIN 12 116	1	2
Alkali resistance class according to DIN 52322	2	3
Dielectric constant ϵ (25°C)	4.7	3.9

	(1MHz)	(40GHz)
$\tan\delta$ (25°C)	$45 \cdot 10^{-4}$	$26 \cdot 10^{-4}$
	(1MHz)	(40GHz)

To produce particular properties in the modules, it may be expedient to use glasses of different compositions for the glass layers on the top side and on the underside. It is also possible for a plurality of glasses having different properties, e.g. with regard to refractive index, density, E modulus, Knoop hardness, dielectric constant, $\tan\delta$, to be deposited successively on the substrate.

As an alternative to electron beam deposition, it is also possible to use other means for transferring materials which are deposited in glass form. For example, the vapor-coating material may be in a crucible which is heated by electron impact heating. Electron impact heating of this type is based on thermionic discharges which are accelerated onto the crucible in order to impact on the material to be vaporized with a predetermined kinetic energy. These processes likewise make it possible to produce glass layers without excessive thermal loading on the substrate on which the glass is deposited.

The following text present results of various tests carried out on vapor-deposited glass layers formed from glass 8329.

Fig. 11 shows the results of a TOF-SIMS measurement, in which the count rate is plotted as a function of the sputtering time. The measurement characterizes the profile of the element concentrations in the direction perpendicular to the substrate surface. A thickness constancy for the glass frame of < 1% of the layer thickness was determined.

Fig. 12 shows an electron microscope transverse microsection image of a silicon substrate coated with the vapor-deposition glass 8329. The vapor-deposition glass and the surface of the silicon substrate are securely bonded to one another in a manner which is not released even by the transverse microsectioning operation involved in preparing the specimen.

Furthermore, resistance and stability measurements were carried out on a vapor-deposition glass layer formed from vapor-deposited glass 8329, in accordance with DIN/ISO. The results are given in Table 1.

Table 1:

Specimen designation: 8329			
<u>Water DIN ISO</u> 719 Class	Consumption of HCl [ml/g]	Na ₂ O equivalent [µg/g]	Comments
HGB 1 <u>Acid DIN 12116</u> Class	0.011 Material removal [mg/dm ²]	3 Total surface area [cm ²]	none Comments/ visible changes
1 W as material <u>Alkali DIN ISO</u> 695 Class	0.4 Material removal [mg/dm ²]	2 x 40 Total surface area [cm ²]	unchanged Comments/ visible changes
A 2 As material	122	2 x 14	unchanged

Patent Claims

1. Process for forming a housing for electronic modules, in particular sensors, integrated circuits and optoelectronic components;

comprising the steps of:

- providing a substrate (1), of which at least a first substrate side (1a) is to be encapsulated,
- providing a vapor-deposition glass source (20),
- 10 - arranging the first substrate side (1a) in such a manner with respect to the vapor-deposition glass source that the first substrate side (1a) can be vapor-coated;
- vapor-coating the first substrate side with a glass layer (4).

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2. The process as claimed in claim 1, wherein the substrate provided has one or more regions comprising semiconductor structures (2) and comprising connection structures or for forming semiconductor structures (2) and connection structures (3).

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3. The process as claimed in claim 2, wherein the one or more regions having semiconductor structures (2) are arranged on the first side (1a) of the substrate.

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4. The process as claimed in claim 3, wherein the substrate is provided with a passivation layer (10, 11) on a second side (1b), which is on the opposite side from the first side (1a).

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5. The process as claimed in one of the preceding claims, the substrate comprising a wafer, wherein the process comprises the packaging of components which still form part of a wafer.

6. The process as claimed in one of the preceding claims, wherein the substrate (1) is vapor-coated with a glass layer (4, 10, 11) on two sides (1a, 1b).

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7. The process as claimed in one of the preceding claims, wherein a vapor-deposition glass source (20) which generates at least a binary glass system is provided.

10 8. The process as claimed in one of the preceding claims, wherein the vapor-deposition glass source (20) is operated until the glass layer (4) has a thickness in the range from 0.01 to 1000 μm , in particular on the first substrate side.

15 9. The process as claimed in one of the preceding claims, wherein as part of the step of providing a vapor-deposition glass source (20), a reservoir comprising organic constituents is provided, and these organic constituents are converted into the vapor state through application of a
20 vacuum or through heating, so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the substrate side.

10. The process as claimed in one of the preceding claims,
25 wherein the glass layer thickness is in the range between 0.1 and 50 μm .

11. The process as claimed in one of the preceding claims, wherein the glass layer thickness is in the range between 50
30 and 200 μm .

12. The process as claimed in one of the preceding claims, wherein the vapor-deposition glass of the source (20) is generated from a glass target (23) by means of electron beam

(24).

13. The process as claimed in one of the preceding claims,
wherein the vapor-deposition glass used is a borosilicate
5 glass containing aluminum oxide and alkali metal oxide
fractions.

14. The process as claimed in one of the preceding claims,
wherein the vapor-deposition glass has a coefficient of
10 thermal expansion which is virtually equal to that of the
substrate.

15. The process as claimed in one of the preceding claims,
wherein the glass layer (4) is produced with a thickness
15 which is required for a hermetic seal, and wherein a layer of
plastic (5) is applied above the glass layer (4) in order to
facilitate further processing of the substrate (1).

16. The process as claimed in one of the preceding claims,
20 wherein a plurality of glass layers are vapor-deposited onto
the substrate (1), it being possible for the glass layers to
consist of various glass compositions.

17. The process as claimed in one of the preceding claims,
25 wherein the further processing of the substrate (1) involves
the removal of material from a second substrate side (1b),
which is on the opposite side from the first substrate side
(1a).

30 18. The process as claimed in one of the preceding claims,
wherein the substrate (1) includes a wafer having a plurality
of semiconductor structures (2) and connection structures
(3), with the second substrate side (1b), which is on the
opposite side from the first substrate side (1a), being
35 thinned, pits (6) being etched on the second substrate side

(1b) in the region of the connection structures to be produced, the regions for forming the semiconductor structures (2) being lithographed using plastic layers, line contacts (7) being produced on the second substrate side (1b) in the regions having connection structures (3), the plastic being removed from the second substrate side (1b), a ball grid array (8) being applied at the line contacts (7), and the wafer being divided up so as to form a plurality of electronic modules which each have first, encapsulated sides (1a).

19. The process as claimed in claim 18, wherein the second substrate side (1b) is provided with a plastic covering (10) while leaving clear the ball grid regions (8).

20. The process as claimed in claim 18 or 19, wherein after the plastic has been removed from the second substrate side (1b) the whole of the second substrate side is vapor-coated with a glass layer (11), and wherein the line contacts (7) are uncovered by local elimination of the glass layer (11), after which the steps of applying the ball grid array (8) and of dividing up the wafer are carried out in order to obtain electronic modules which are encapsulated on both sides.

21. The process as claimed in claim 20, wherein the entire second substrate side is vapor-coated with a glass layer (11) with a thickness in the range from 1 to 50 μm , and

22. The process as claimed in one of claims 18 to 21, wherein the etching pits (6) which lead to the connection structures (3) are filled with conductive material (12), after which, with or without removal of the plastic (10) from the second substrate side (1b) and with or without a glass

layer (11) on the second substrate side (1b), and leaving clear the line contacts (7), the ball grid array (8) is applied at the line contacts (7) and/or at the filling material.

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23. The process as claimed in one of the preceding claims, wherein the vapor-coating of the first substrate side (1a) with a glass layer (4) comprises plasma ion assisted deposition (PIAD).

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24. An electronic module, in particular as a sensor or as an integrated circuit or as an optoelectronic component, producible by the process as claimed in one of the preceding claims.

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25. The electronic module as claimed in claim 24, which on a first side (1a) has one or more regions with semiconductor structures (2), and connection structures (3), wherein the substrate is coated with a vapor-deposited glass layer (4) on at least one side.

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26. The electronic module as claimed in claim 25, wherein a plastic layer (5) which reinforces the module is applied to the glass layer (4).

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27. The electronic module as claimed in one of claims 25 or 26, wherein the substrate is thinned.

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28. The electronic module as claimed in one of claims 25 to 27, wherein the substrate is provided with a passivation layer (10, 11) on a second side (1b), which is on the opposite side from a first side (1a) having semiconductor structures and connection structures.

29. The electronic module as claimed in one of claims 25 to 28, wherein the glass layer (4) comprises a mixed layer of inorganic and organic constituents.

5 30. The electronic module as claimed in one of claims 25 to 29, which includes a multilayer glass layer (4).

31. The electronic module as claimed in claim 30, wherein the individual layers of the glass layer have different
10 compositions.

32. The electronic module as claimed in one of claims 25 to 31, wherein the substrate (1), on a second side (1b), has line contacts that are connected to connection structures on
15 the first side (1a).

33. The electronic module as claimed in claim 32, which includes a ball grid array (8) at the line contacts.