

The diagram illustrates the internal architecture of a semiconductor memory device (1003) and its interface with a memory controller (1002).

Memory Controller (1002): A vertical block on the left that manages memory operations. It sends control signals (CLE, ALE, WEn, REn) and address/data signals (ADD, DAT, RBN) to the memory device. It also receives a feedback signal (RBN) and is connected to power rails (Vcc, Vss).

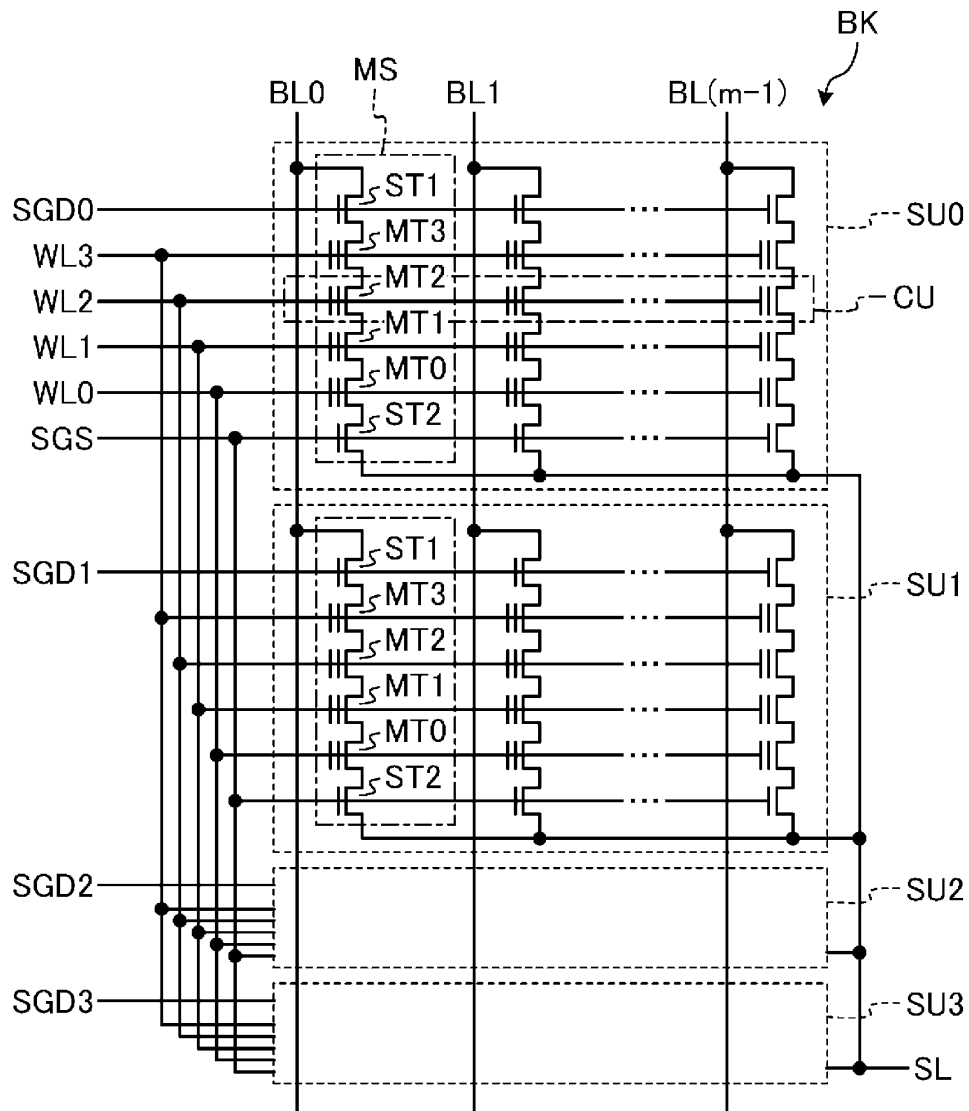
Semiconductor Memory Device (1003): The main block on the right, containing several sub-components:

- 1014 (シーケンサ - Sequencer):** Receives the CMD signal and coordinates the internal operations.
- 1015 (電圧発生回路 - Voltage Generation Circuit):** Generates internal voltages based on the ADD signal and provides them to the sense amplifier and memory array.
- 1016 (電源回路 - Power Circuit):** Manages the power supply, receiving Vcc and Vss signals and providing internal power to the sense amplifier and memory array.
- 1013 (センスアンプ - Sense Amplifier):** Amplifies data from the memory array and outputs it to the DAT bus.
- 1012 (ローデコーダ - Row Decoder):** Receives the ADD signal and activates the word line (WL) for the selected memory row.
- 20 (メモリセルアレイ - Memory Cell Array):** The core of the device, containing multiple memory blocks (BK0, BK1, ..., BK(n-1)). It is connected to the word line (WL) and the sense amplifier.

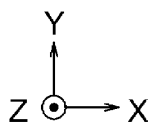
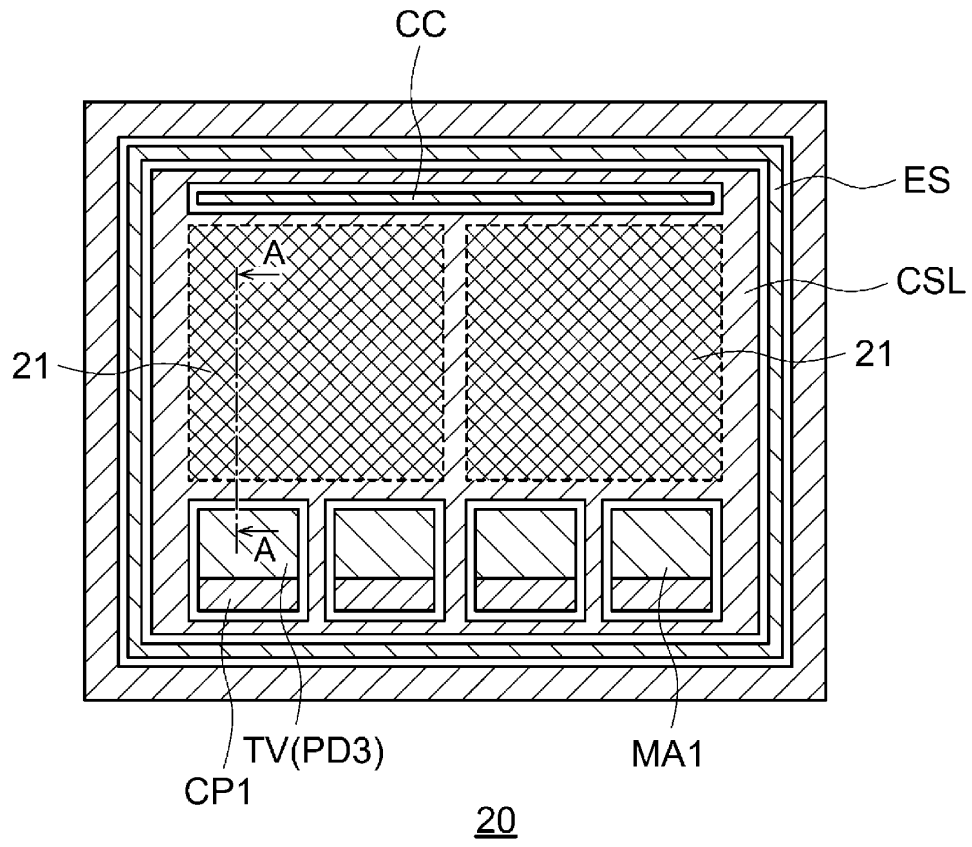
Signal Flow:

- Control Signals:** CLE, ALE, WEn, REn from the controller to the device.
- Address and Data Signals:** ADD and DAT are bidirectional signals between the controller and the device's sequencer and sense amplifier.
- Power Signals:** Vcc and Vss are provided from the controller to the device's power circuit.
- Internal Signals:** The sequencer (1014) sends signals to the voltage generation circuit (1015) and the sense amplifier (1013). The voltage generation circuit (1015) sends signals to the sense amplifier (1013) and the memory array (20). The sense amplifier (1013) sends signals to the memory array (20) and the row decoder (1012). The row decoder (1012) sends signals to the memory array (20).

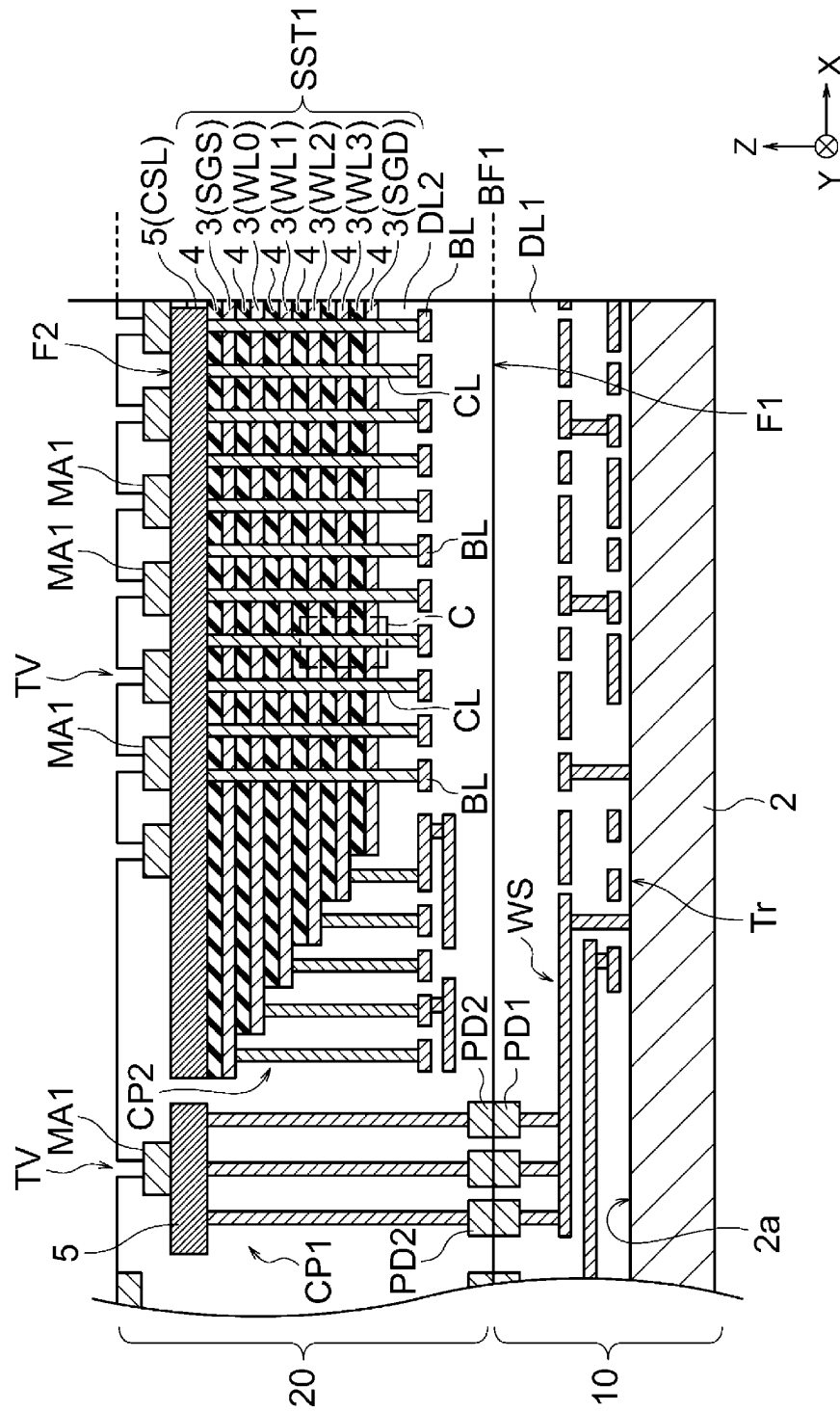
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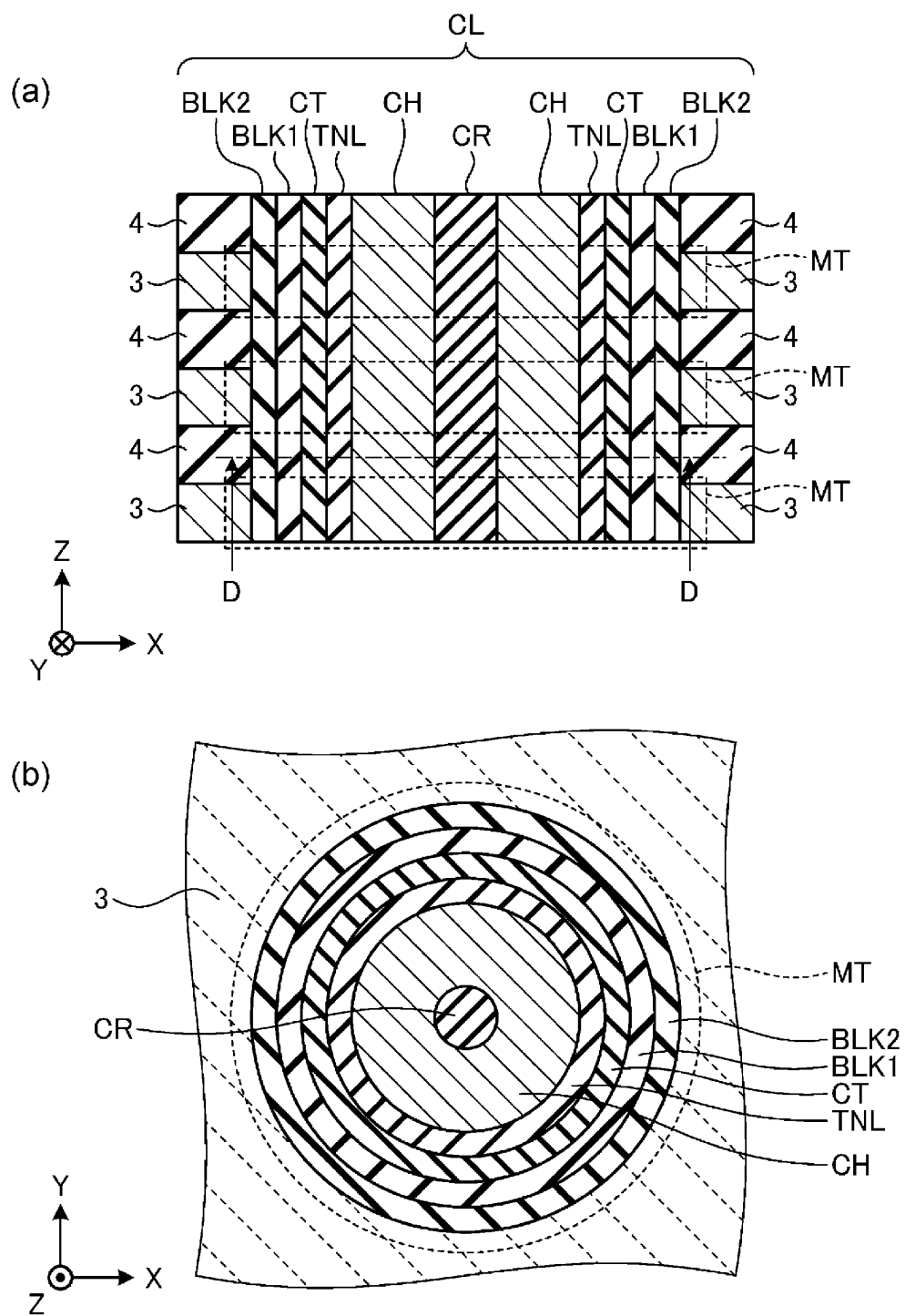
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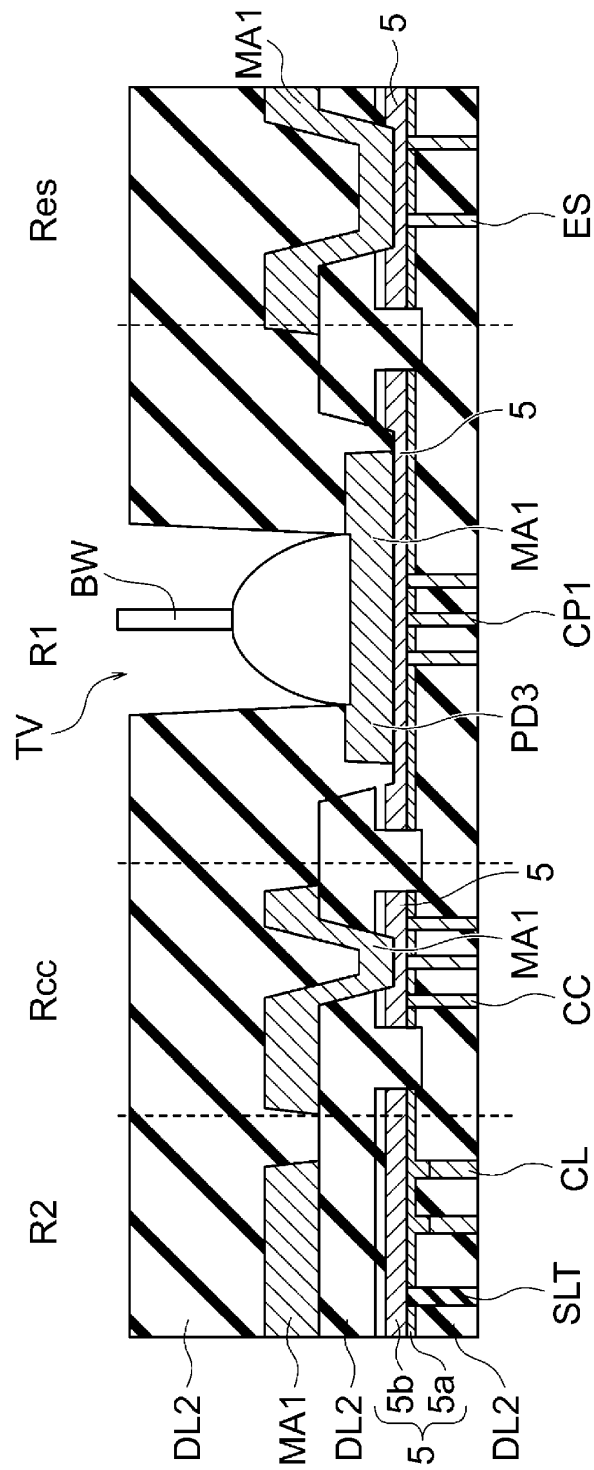
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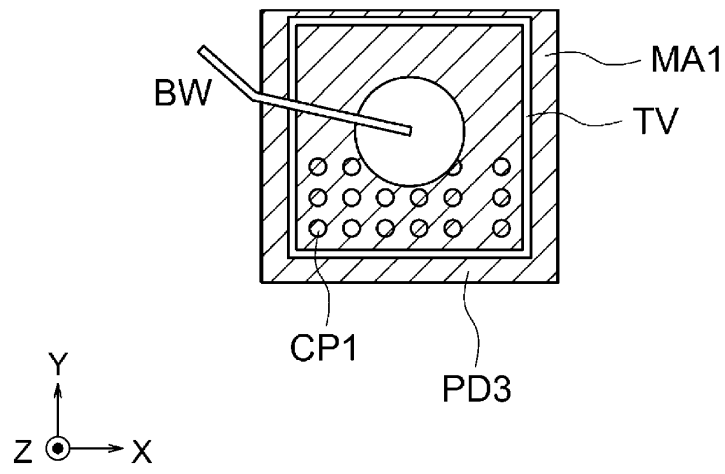
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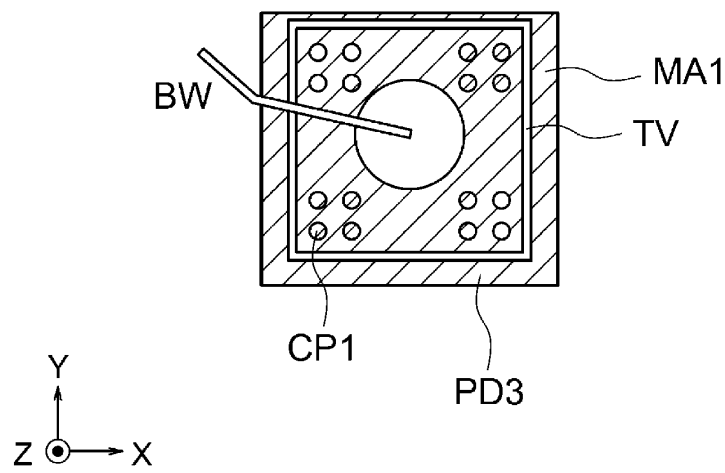
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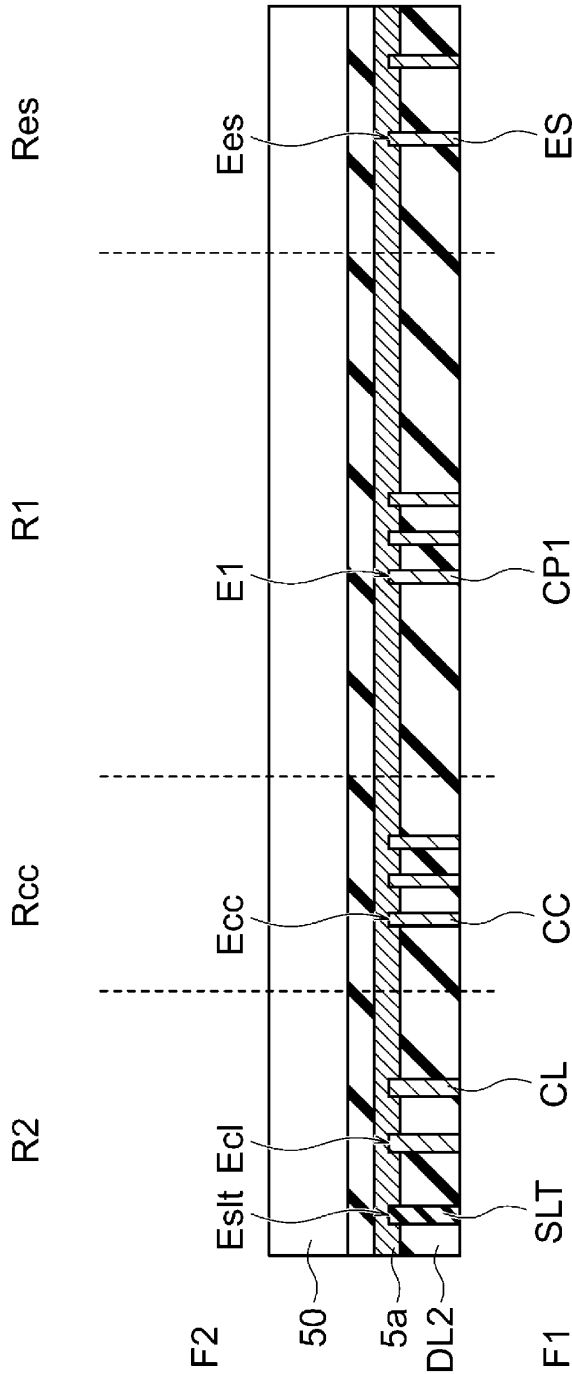
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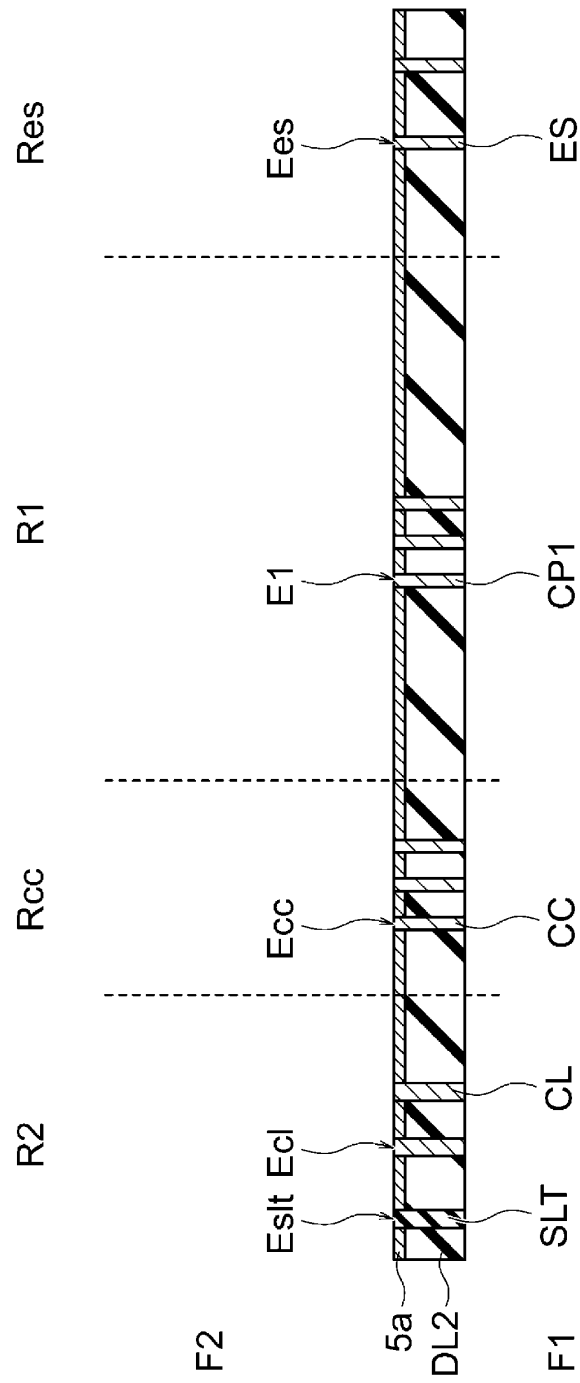
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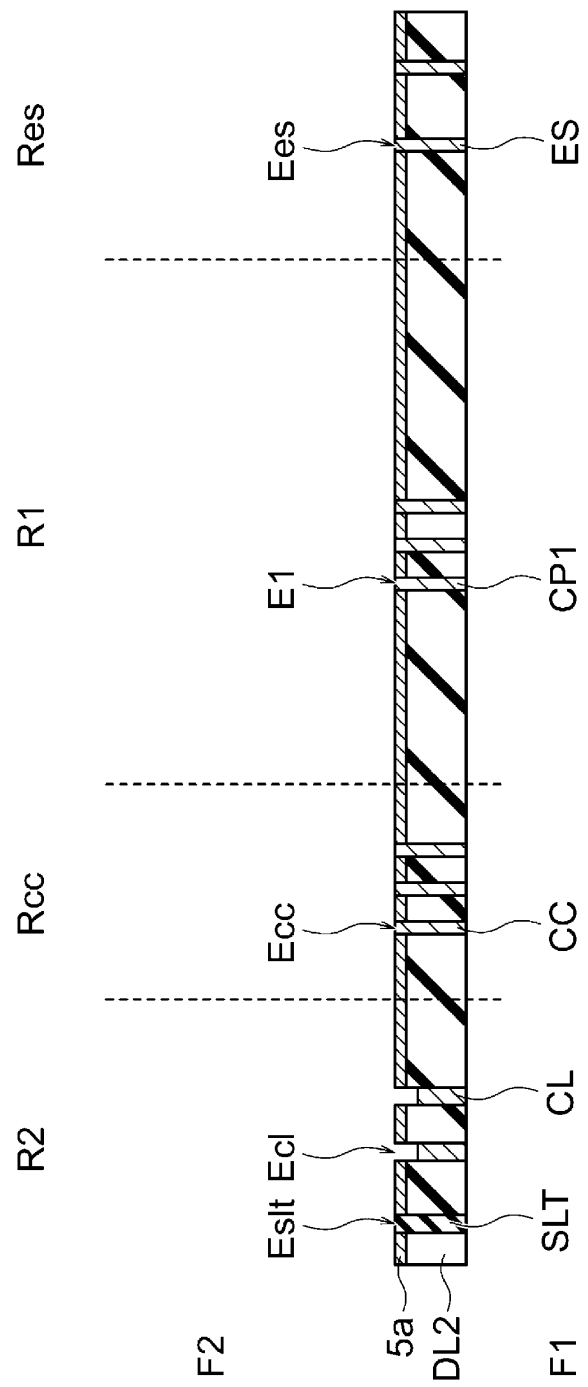
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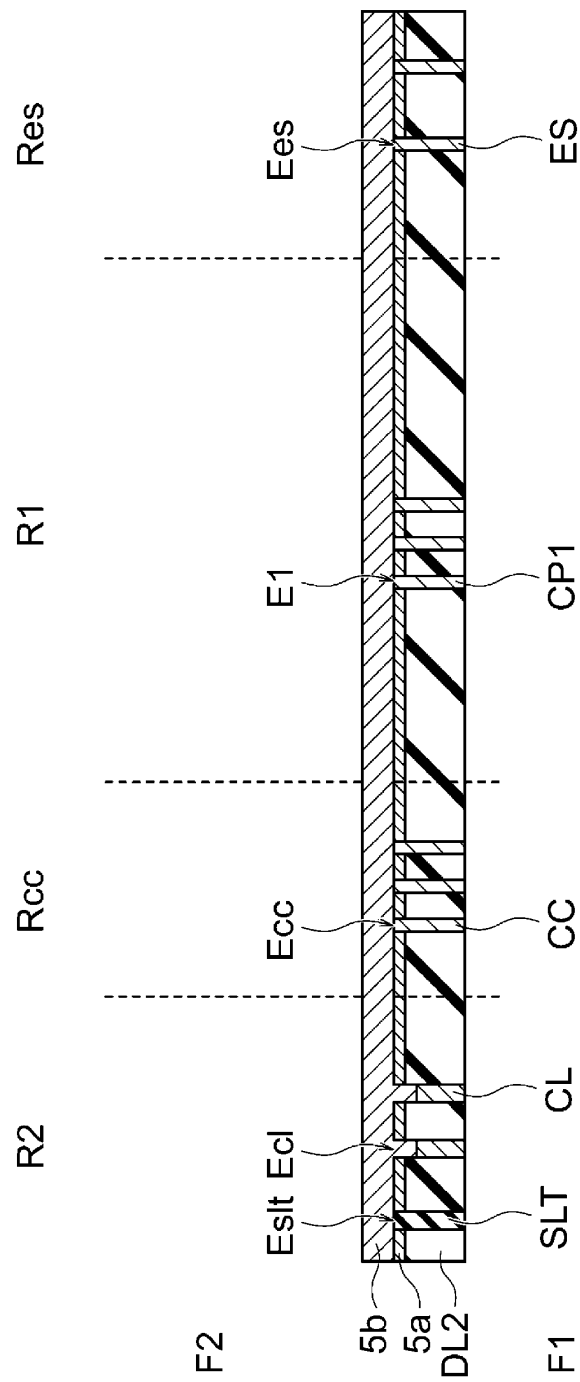
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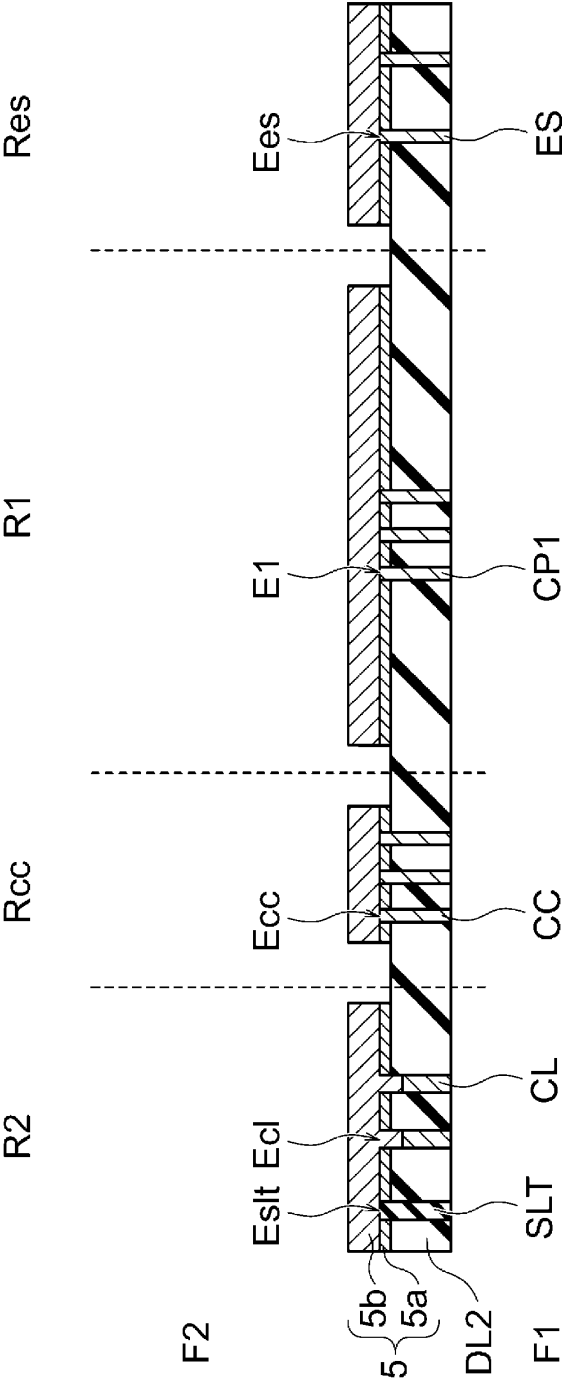
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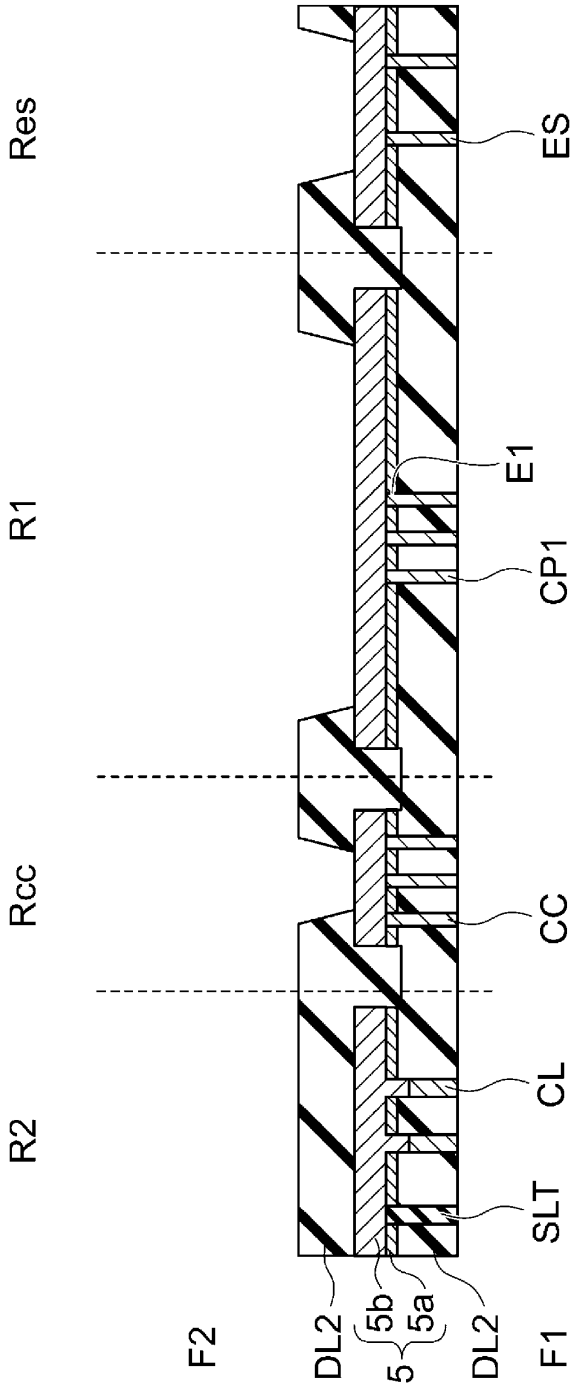
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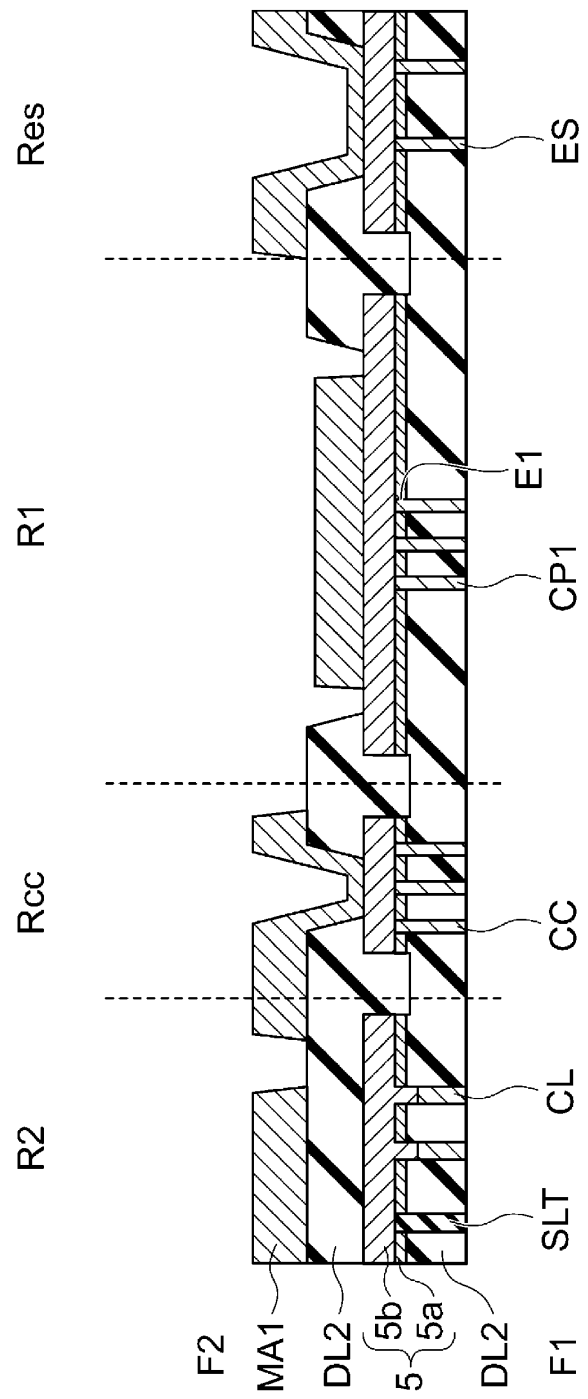
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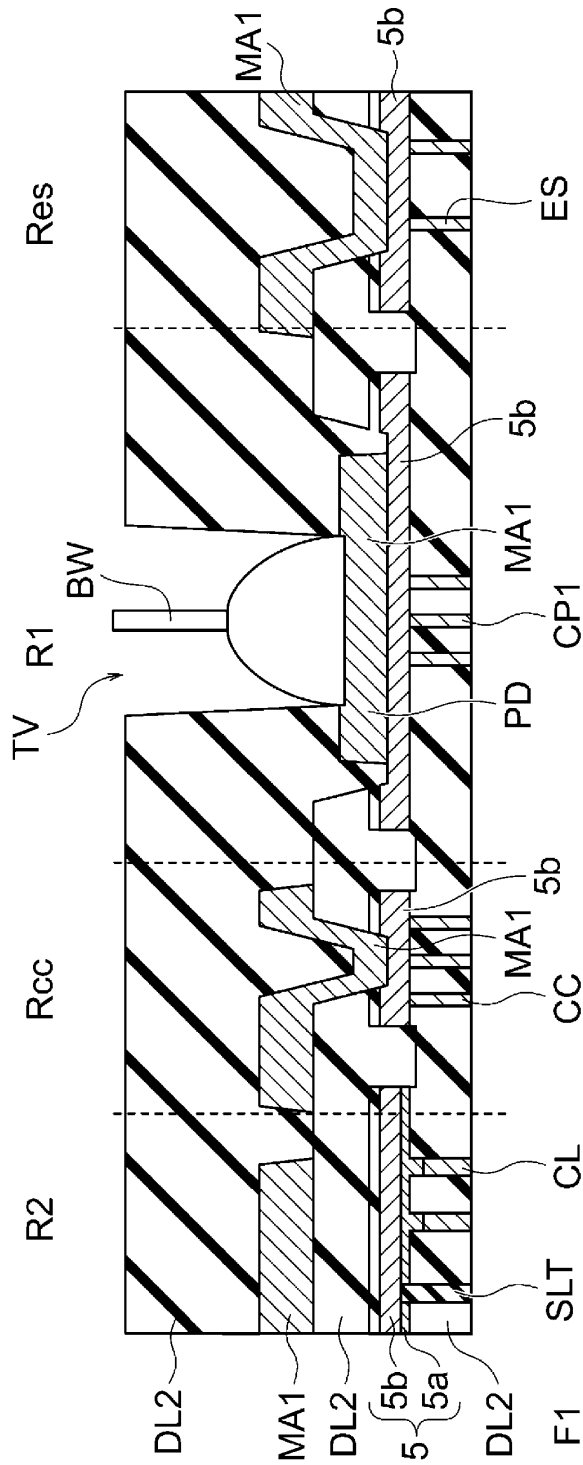
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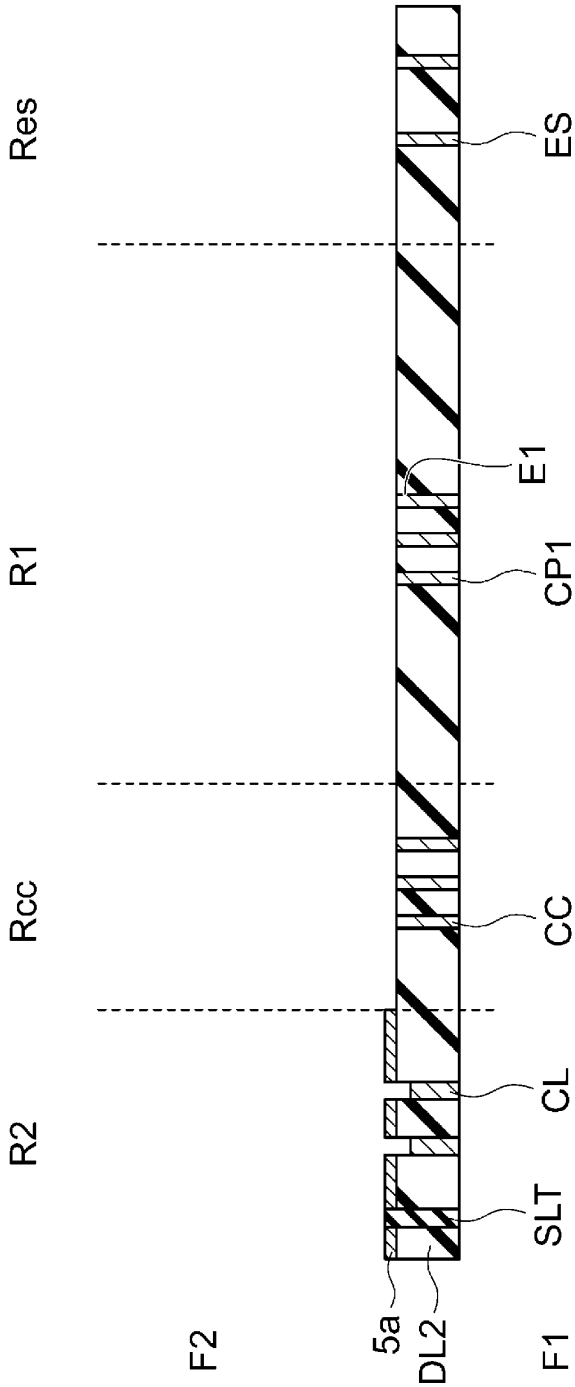
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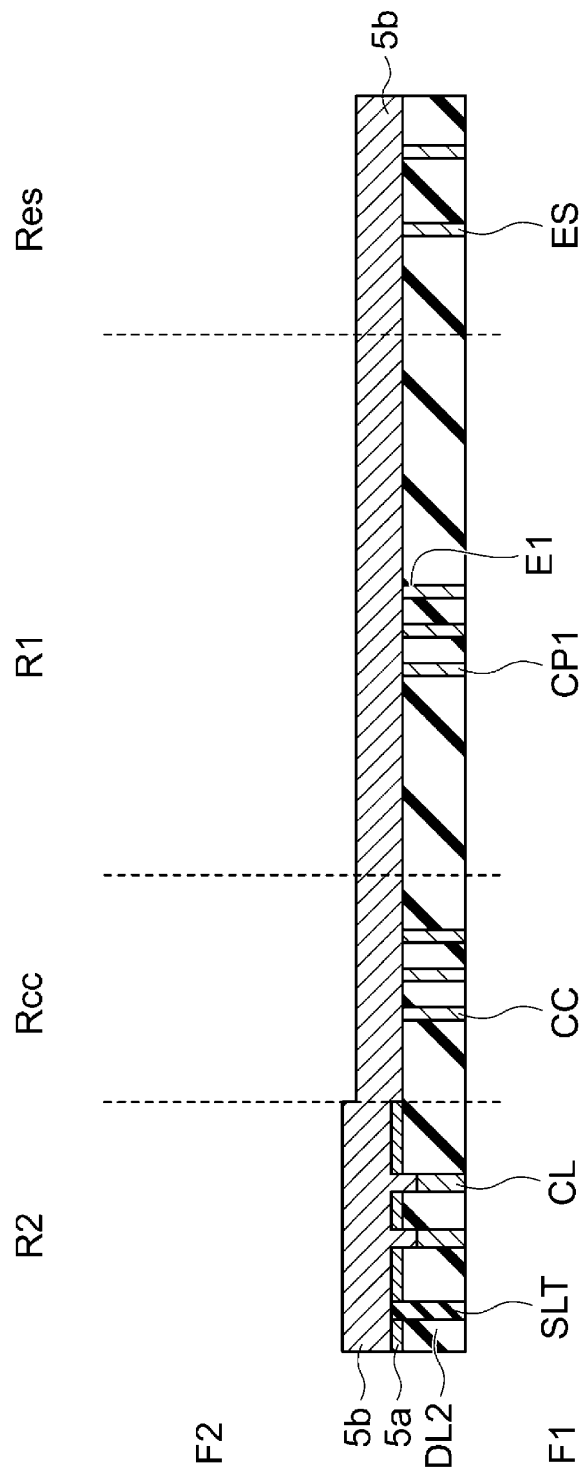
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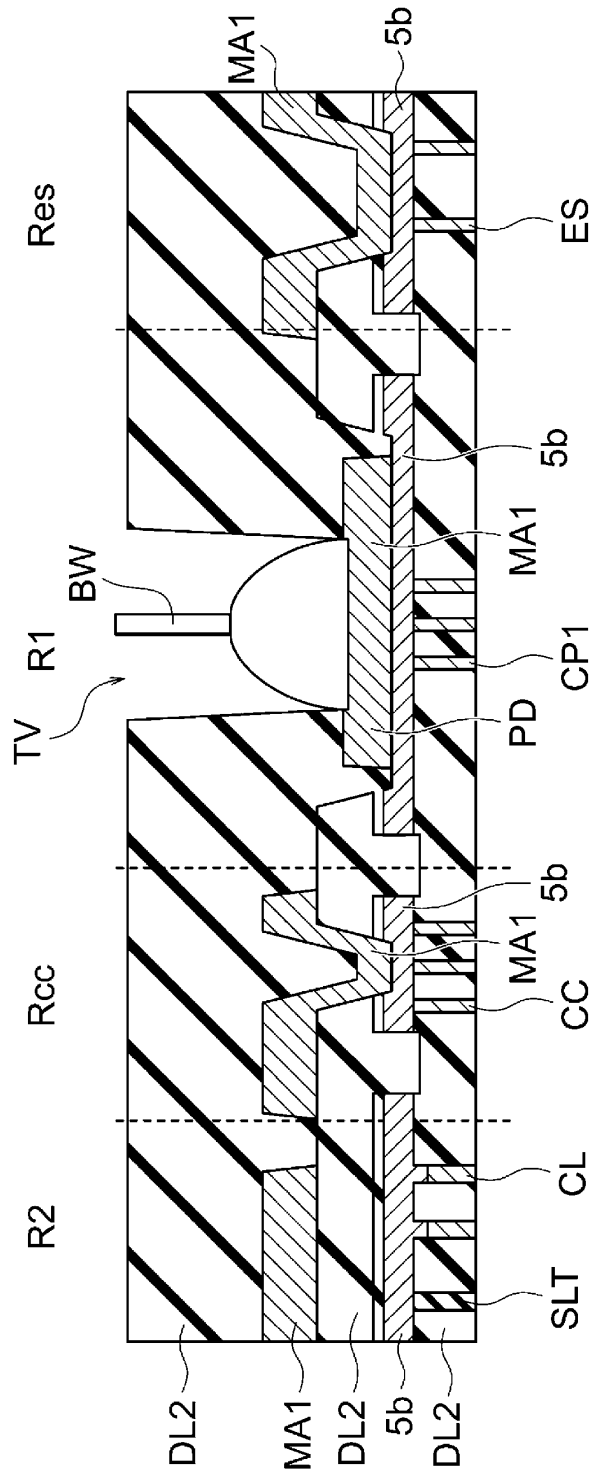
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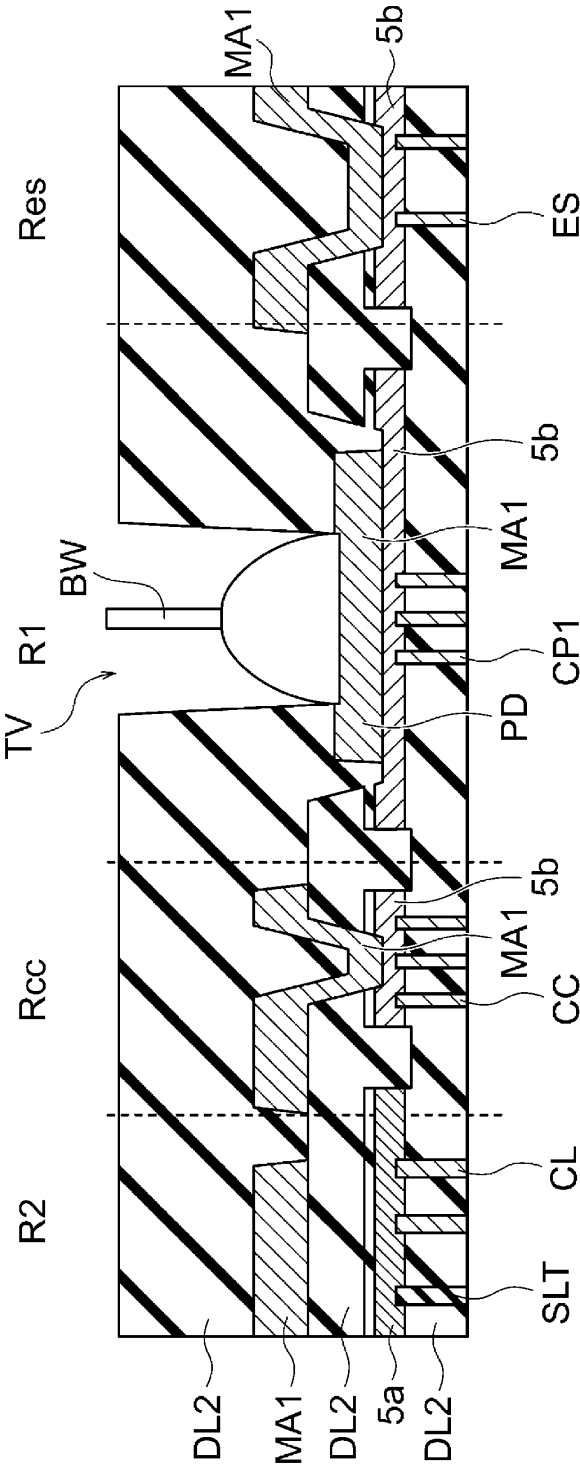
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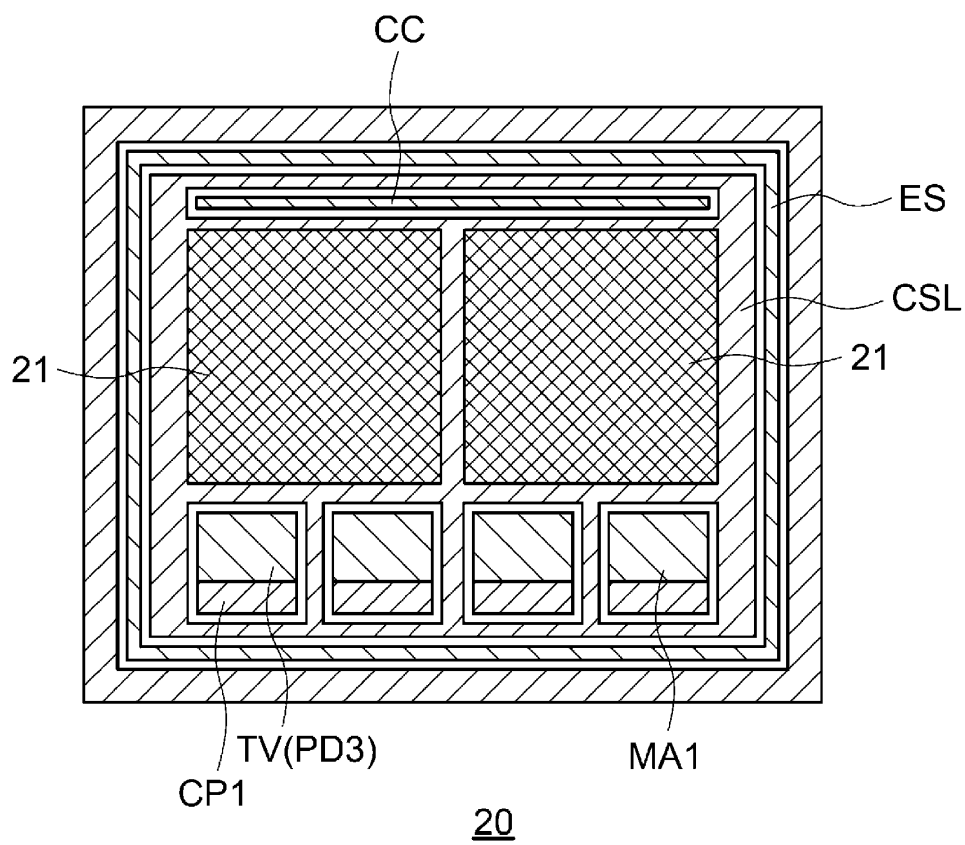
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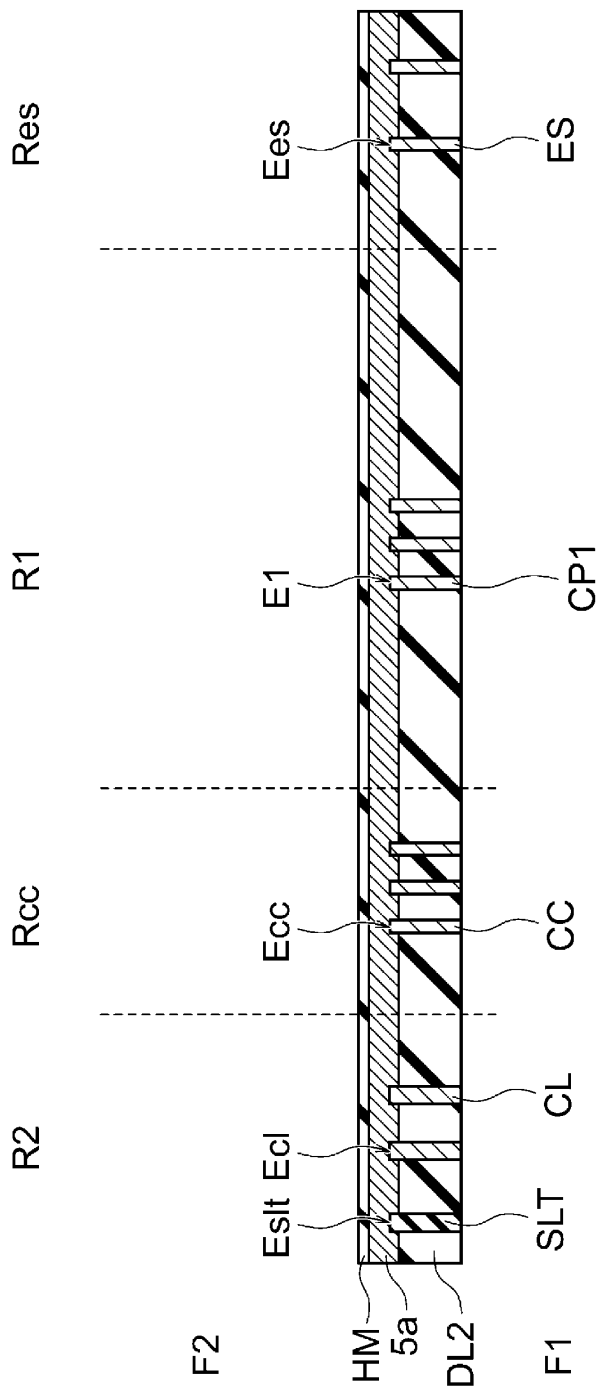
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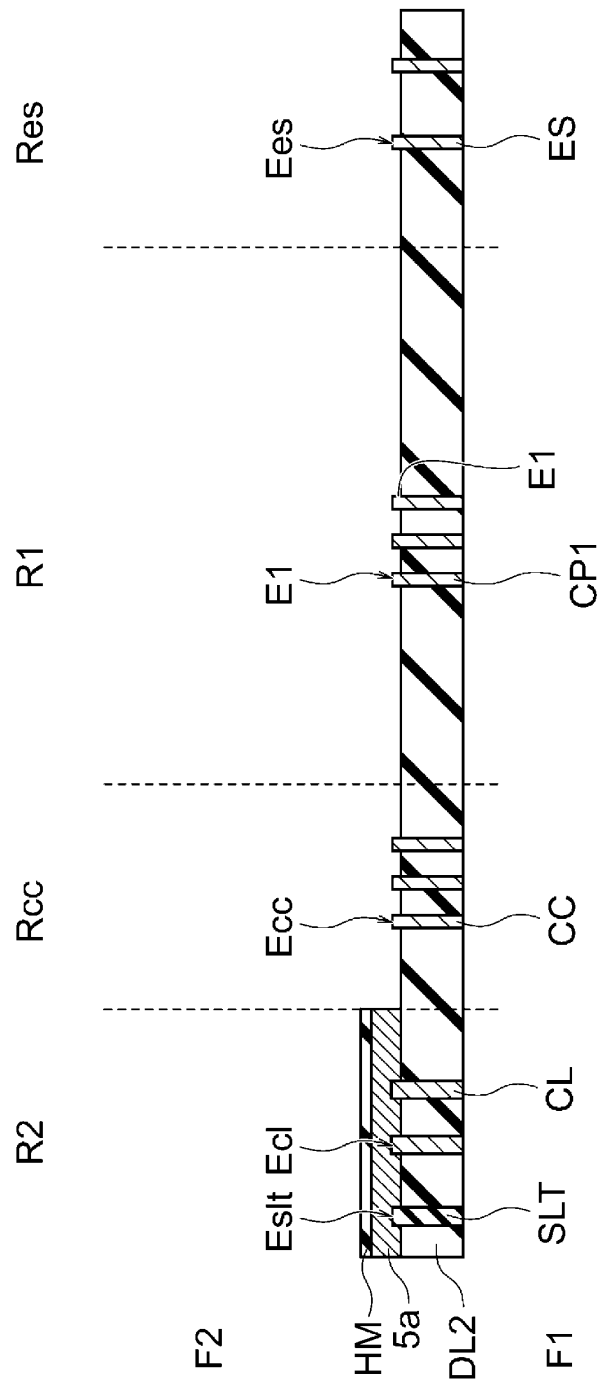
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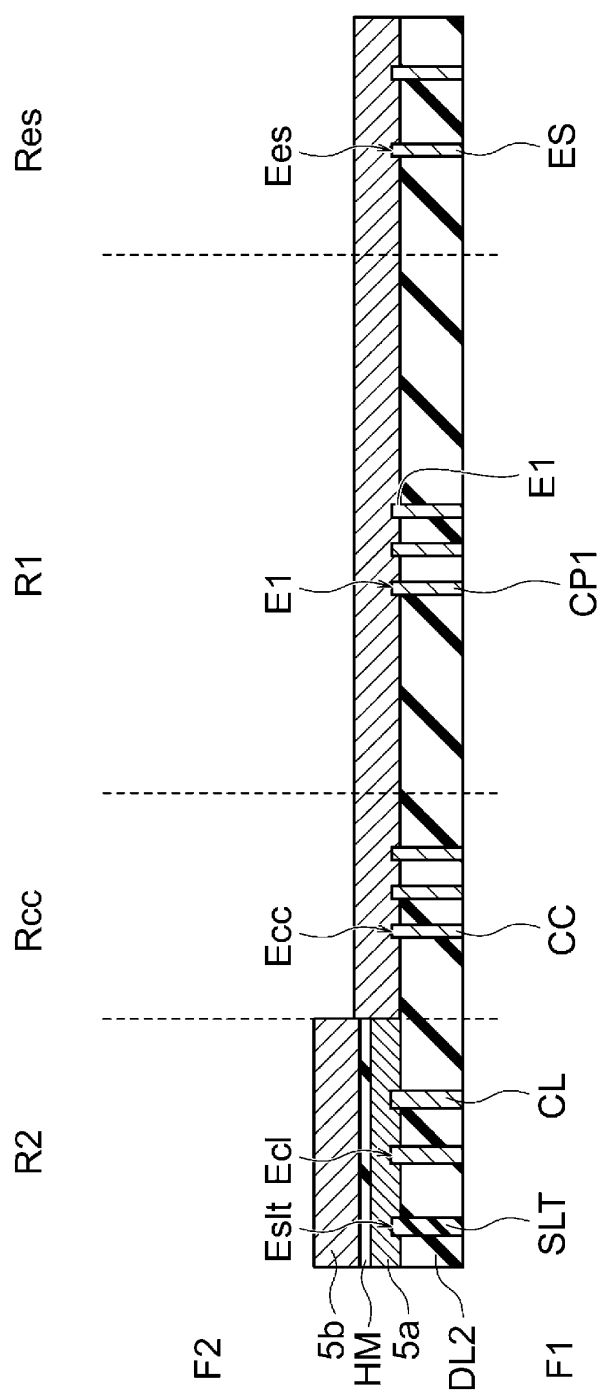
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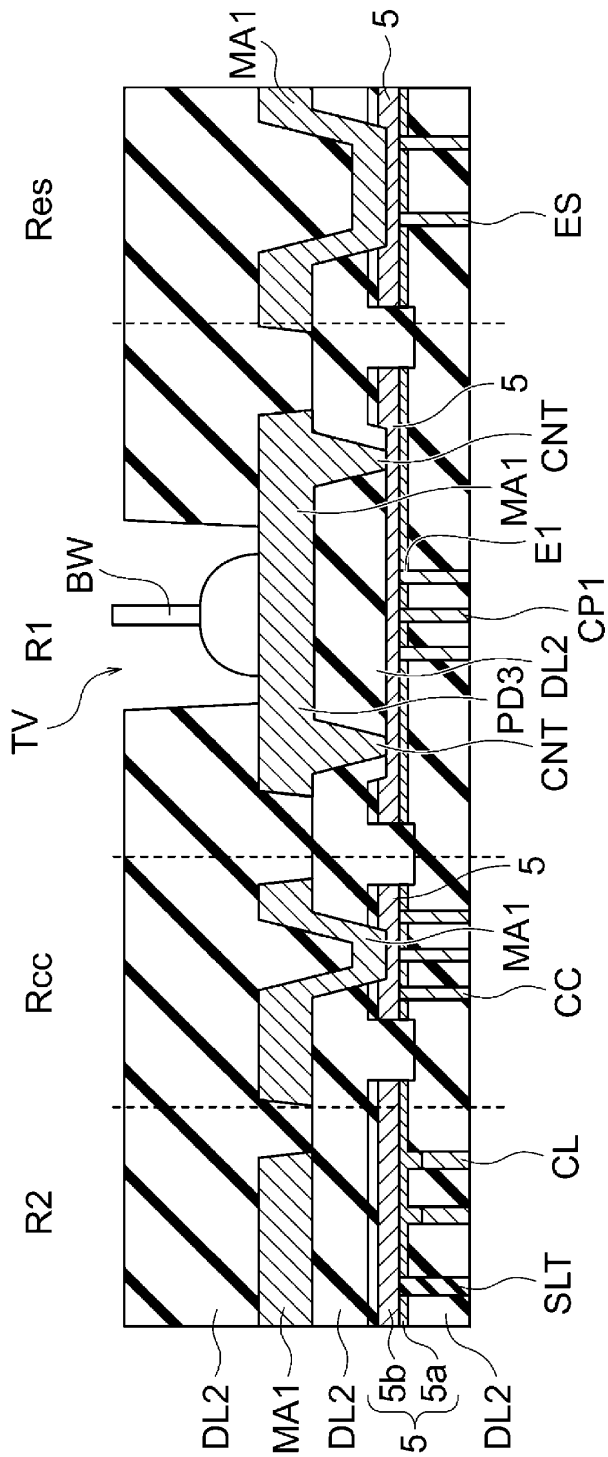
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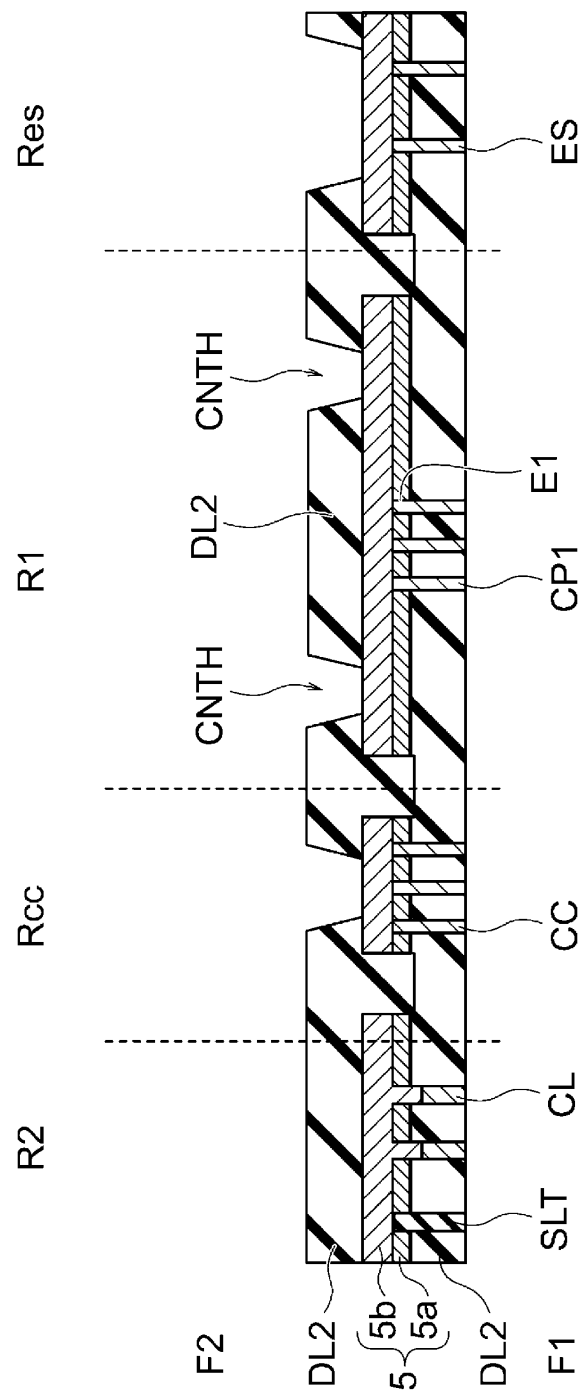
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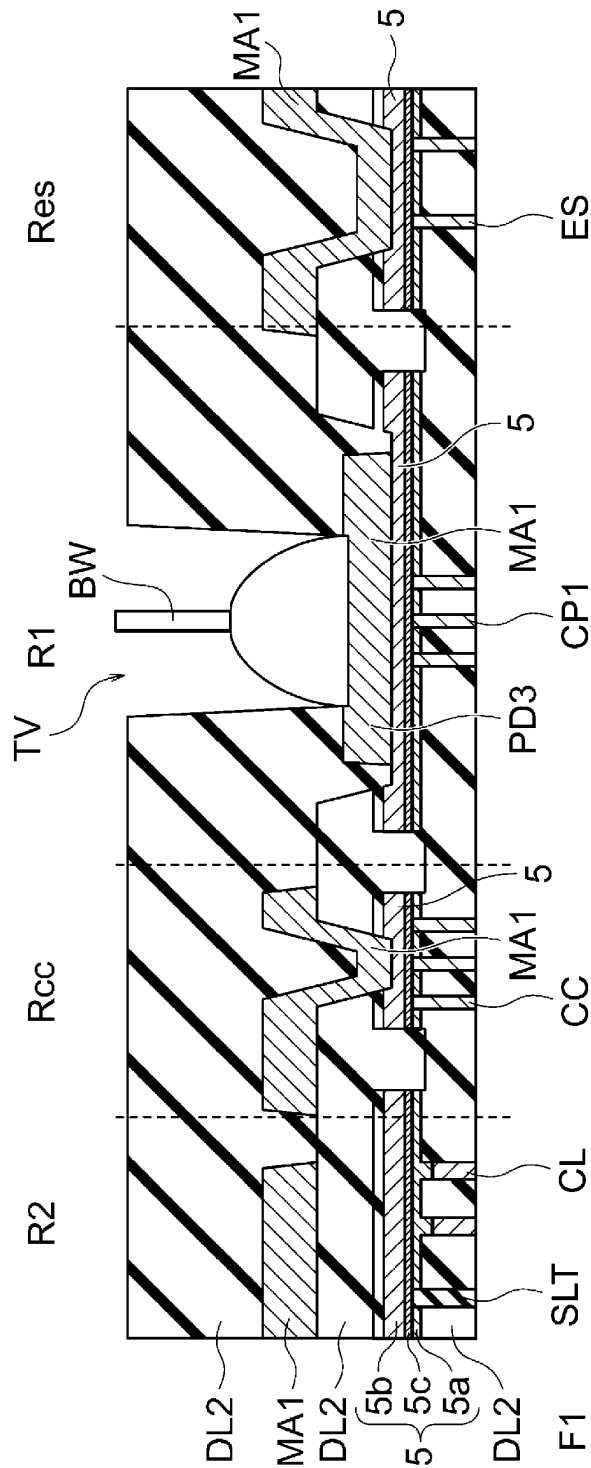
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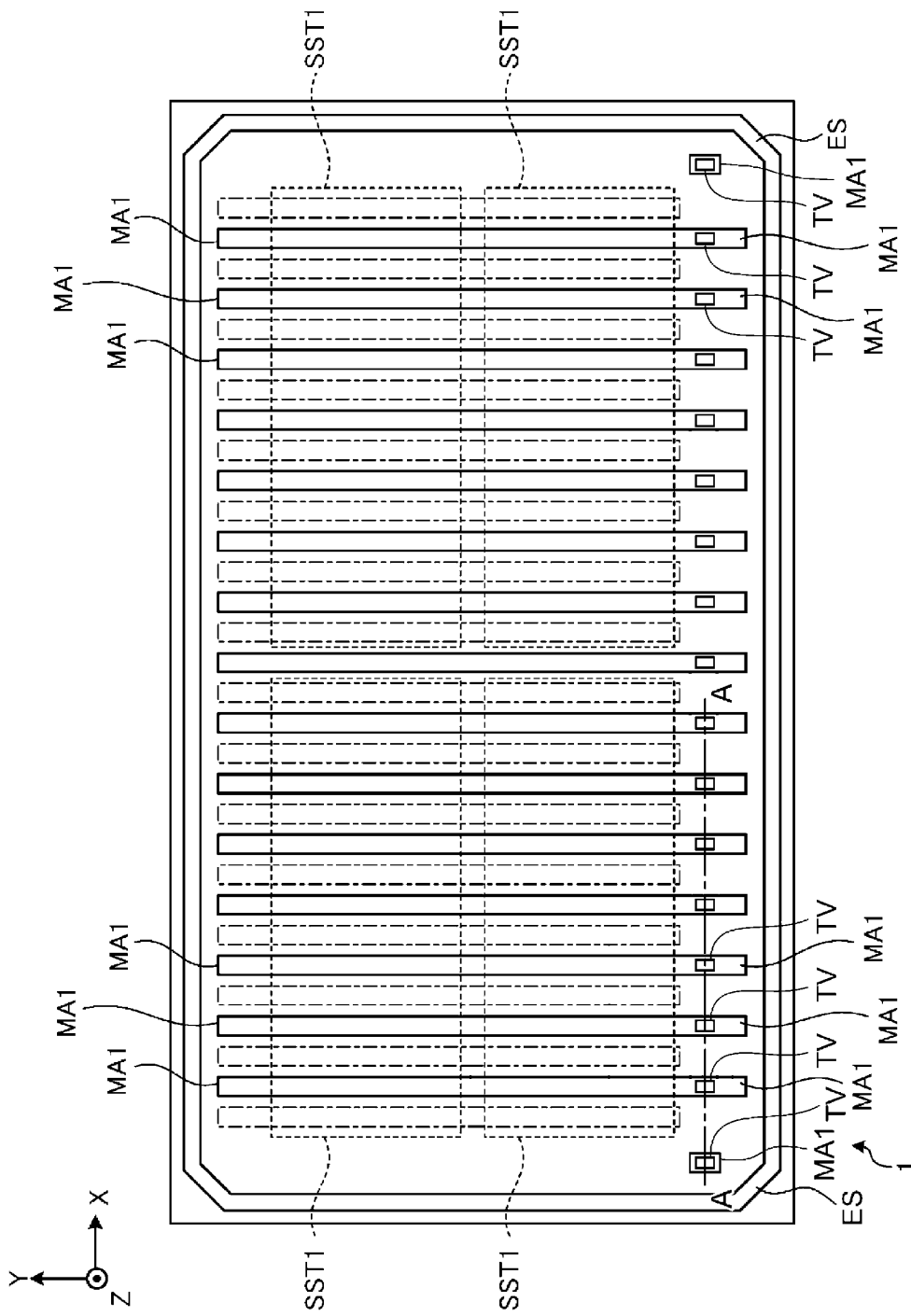
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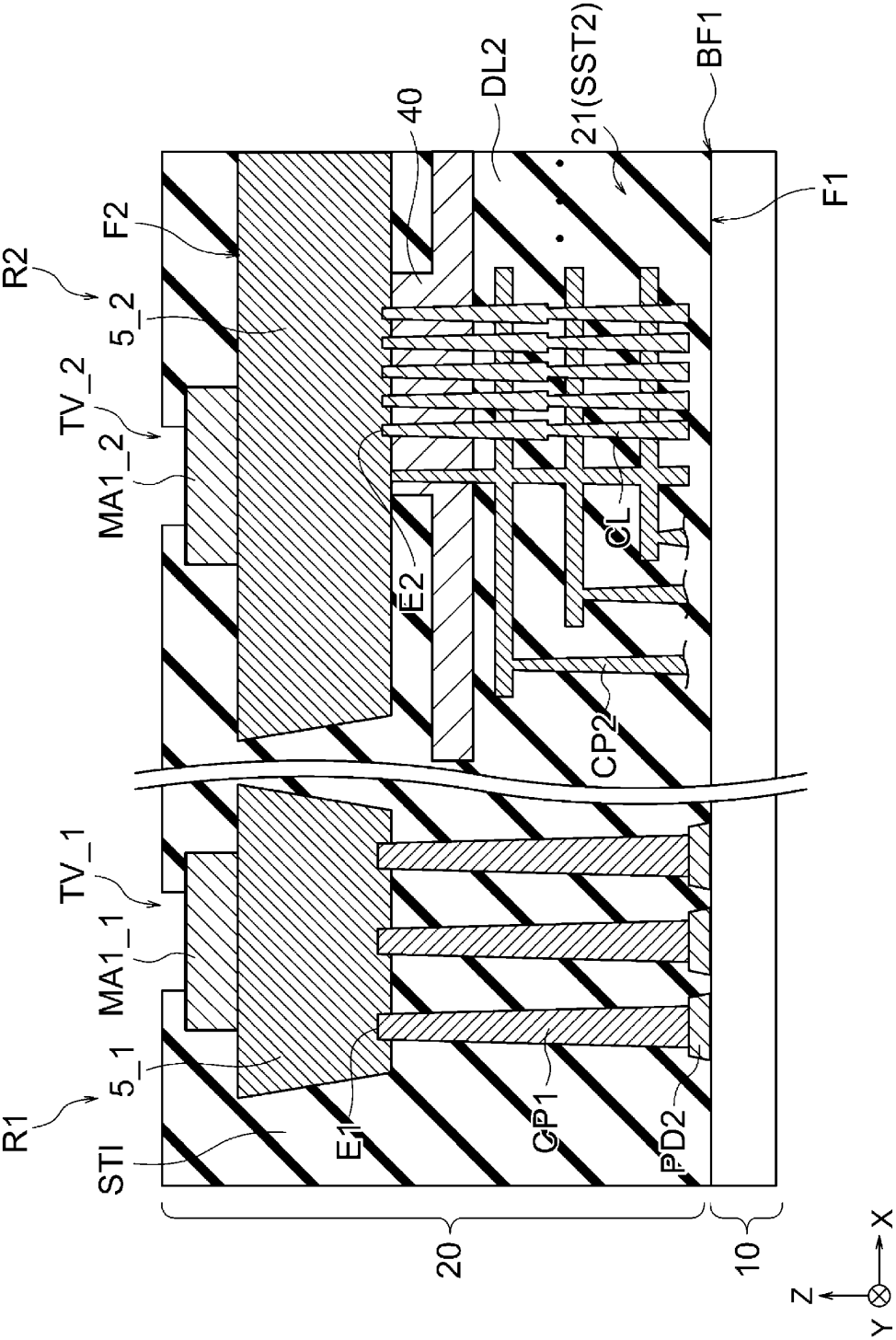
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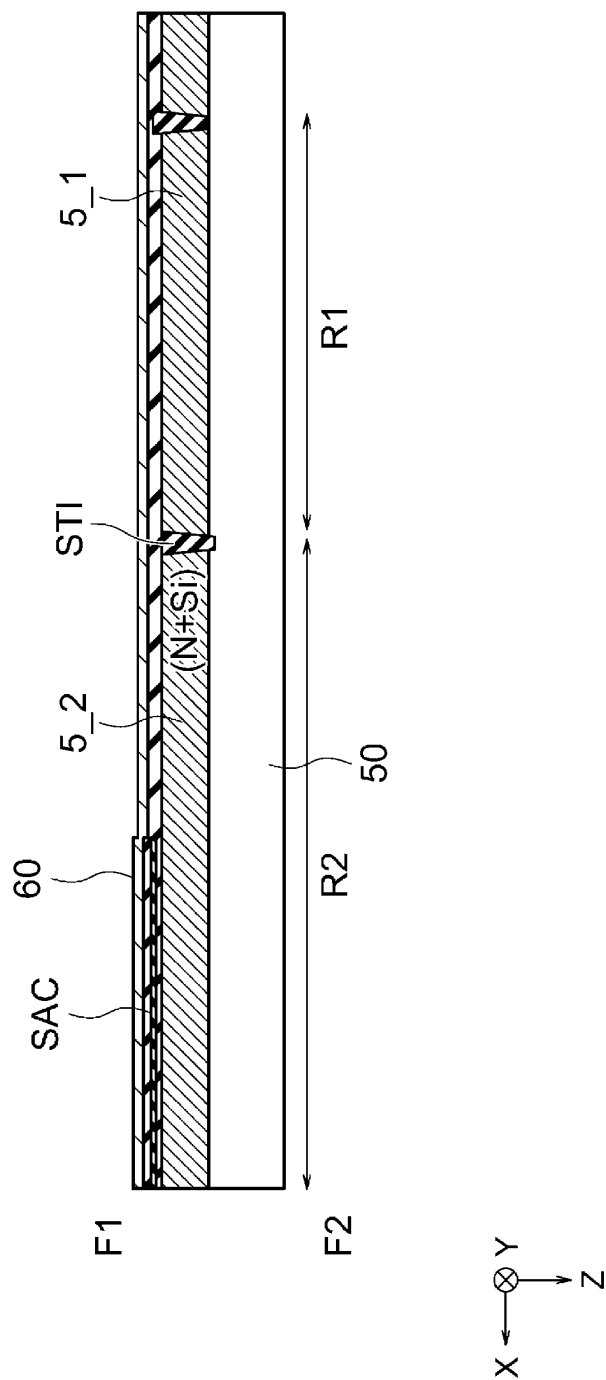


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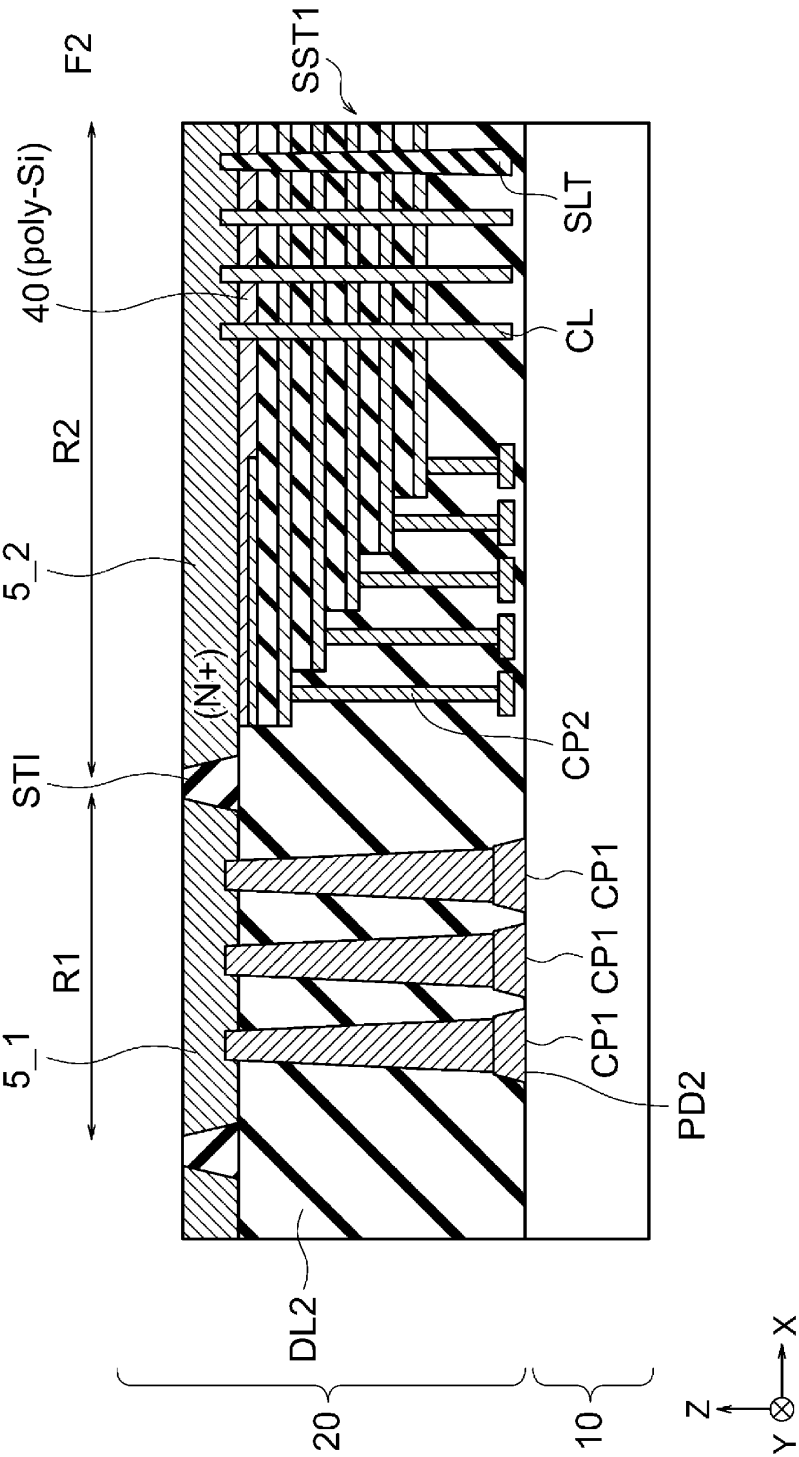


[図30]





[図35]



[図38]

	R 2	Rcc、R1、Res
1	Ti/TiN/W	Ti/TiN/W
2	Ti/TiN/W	Ti(poly)/TiN/W
3	Ti/TiN/W	poly/Ti/TiN/W
4	Ti(poly)/TiN/W	Ti/TiN/W
5	Ti(poly)/TiN/W	Ti(poly)/TiN/W
6	Ti(poly)/TiN/W	poly/Ti/TiN/W
7	poly/Ti/TiN/W	Ti/TiN/W
8	poly/Ti/TiN/W	Ti(poly)/TiN/W
9	poly/Ti/TiN/W	poly/Ti/TiN/W
10	poly(BSL)	Ti/TiN/W
11	poly(BSL)	Ti(poly)/TiN/W
12	poly(BSL)	poly/Ti/TiN/W