Method for finishing a substrate of the semiconductor-on-insulator type.

The invention generally relates to the manufacturing of substrates intended for applications in the fields of electronics, optics and optoelectronics.

More specifically it relates to a method for finishing a substrate known under the acronym of SeOI, ("*Semiconductor On Insulator*").

The invention finds particular application in the finishing of a "SOI" substrate, wherein the semiconductor is silicon.

Among the different manufacturing methods used, mention may be made of those using steps for bonding and transferring layers. An example of such a method is described hereafter.

According to this method, an embrittlement area is generated within a first so-called "donor" substrate, covered with an insulating layer, for example by implantation of atomic and/or ionic species. This substrate is then adhered by molecular adhesion to a second so-called "receiver" substrate.

Next, the donor substrate is separated in two portions, along this embrittlement area, for example by detachment annealing ("exfoliation" or "splitting") so

that an intended thickness of the material of the donor substrate as well as the insulator layer are transferred onto the receiver substrate.

Reference may for example be made on this subject to the method known under the registered trade mark "Unibond" of the applicant.

The appended Fig. 1 is a graphic illustration of a photograph taken with a scanning electron microscope which shows a sectional view of the edge of an SOI substrate, immediately after its detachment annealing. This SOI substrate comprises a buried insulator layer 2 between a silicon support 1 and a surface silicon layer 3. It is clearly seen that the side edge 20 of the insulator layer 2 (here silicon oxide) is potentially widely exposed to chemical etching.

Now, additional treatments are frequently carried out on such an SOI (or SeOI) substrate notably for improving its surface condition, in particular for reducing its roughness or for strengthening the adhesive bond between two layers. Such treatments often involve chemical etching, for example with hydrofluoric acid (HF).

Such a treatment applied to an SOI substrate, as the one illustrated in Fig. 1, results in delamination of the substrate by side etching of the insulator layer 2.

In order to overcome this problem, a method for treating an SOI substrate with Rapid Thermal Annealing (known as "RTA" to the person skilled in the art) is known from document US 6,939,783, this treatment having the effect of generating a side encapsulation of the edge of the silicon oxide layer 2 with the silicon located above.

The appended Fig. 2 is a graphic illustration of a photograph taken with a scanning electron microscope which shows a transverse sectional view of the edge of an SOI substrate at the end of such a treatment. As this may be seen, the silicon of the surface layer 3 of the SOI is moved and covers the side edge 20 of the silicon oxide 2 by protecting the latter. This encapsulation portion is referenced as 30.

Now, the applicant carried out tests and unfortunately noticed that the expected protective beneficial effects of the encapsulation were not always obtained since the edge of the transferred silicon layer 3 may have irregularities relatively to the ideal case illustrated in Fig. 2.

The applicant discovered that defects, present at the edge of a SeOI or SOI substrate and although being part of an exclusion area, within which no electronic component will be produced, may perturb the encapsulation phenomenon.

Among the latter, a first type of defects designated as "flakes" is formed by pieces of the substrate which have appeared during detachment and which have been detached and then again notably adhesively bonded onto the edge of the substrate.

Such flakes 31 are visible in the appended Fig. 3, which schematically illustrates an SOI substrate seen as a transverse sectional view.

A second type of defects called "jagged edge" is formed by extensions of the surface of the upper layer of silicon beyond the usual edge of the transferred surface.

Such defects 32 are visible in the aforementioned Fig. 3 and in the appended Fig. 4 which is a graphic illustration of a photograph taken with a

scanning electron microscope, of an SOI substrate edge as seen from above.

The applicant thus discovered that the obtained encapsulation, when it is achieved by an RTA treatment, may be perturbed, notably be too thin at the top of the jagged edges 32. When this encapsulation is carried out by epitaxy treatment, it may also be perturbed, or even completely anarchical at the flakes 31 on which a larger amount of encapsulation material may be formed, with for example the formation of material excrescences.

The encapsulation may even not be complete depending on the shape of the irregularities present at the edge of the substrate (plate edge), and consequently certain portions of the buried insulator may remain accessible to chemical etching for example with hydrofluoric acid (HF).

Moreover, certain flakes or jagged edge pieces may be detached from the receiver substrate before the encapsulation and be redeposited on the surface layer 3 of the SeOI substrate, and then be definitively sealed by the encapsulation, thereby generating defects on this layer.

The appended Fig. 5 is an illustration of a photograph taken with a scanning electron microscope of a substrate of the SOI type, on which this poor quality encapsulation may be observed, and notably the portion of the poorly encapsulated buried insulator which has undergone etching by hydrofluoric acid.

The object of the invention is therefore to solve the aforementioned drawbacks of the state of the art.

The object of the invention is notably to provide a method for finishing a substrate of the SeOI type with which it is possible to have very good

quality encapsulation of the side edge of the buried insulator, i.e. a homogeneous encapsulation, such that the side edge of the insulator is covered over its totality with a layer of semiconducting material with a relatively constant thickness and the edge of this layer forms a regular crown at a constant distance from the edge of the plate.

For this purpose, the invention relates to a method for finishing a substrate of the semiconductor-on-insulator (SeOI) type comprising an insulator layer buried between two layers of semiconducting material.

According to the invention, this method successively comprises:

- routing of the annular periphery of said substrate so as to obtain a routed substrate,
- encapsulation of the routed substrate so as to cover the routed side edge of said buried insulator layer, by means of a semiconducting material.

According to other advantageous and non-limiting features of the invention, taken alone or as a combination:

. the encapsulation of the routed substrate is carried out immediately after routing,

. the routing is carried out by grinding of the peripheral annular edge of said SeOI substrate,

. the routing is carried out by etching of the peripheral annular edge of said SeOI substrate,

. the encapsulation of the routed substrate is carried out by submitting it to a rapid thermal annealing (RTA) treatment,

. the rapid thermal annealing (RTA) treatment is conducted at a temperature comprised between 1,150°C and 1,300°C, for a duration comprised between 15 seconds and about 5 minutes,

. the rapid thermal annealing (RTA) treatment is conducted under an atmosphere of hydrogen and/or argon,

. the step for encapsulating the routed substrate is carried out by epitaxy,

. the step for encapsulating the routed substrate is carried out by a rapid thermal annealing (RTA) treatment and by epitaxy,

. the step for encapsulating the routed substrate is carried out by annealing with a laser,

. the routing comprises the steps of:

- depositing a layer of a protective material on a peripheral annular area of said SeOI substrate, by means of a plasma,

- achieving partial etching of said protective material by means of a plasma, so as to keep a ring of protective material on the front face of said SeOI substrate, this ring extending at a distance from the side edge of said substrate, and to thereby delimit a reduced peripheral annular area of said substrate accessible to a plasma,

- generating a partial etching plasma, localized at said reduced peripheral annular area of the SeOI substrate, so as to etch the material present in this area over a certain thickness,

- removing said ring of protective material by means of a plasma.

. the routing is carried out in an enclosure for forming an isotropic plasma.

. the routing is carried out by steps consisting of:

- introducing said SeOI substrate inside an enclosure for forming an isotropic plasma, equipped with an upper disk-shaped insulating element and with two electrodes, one of them a so-called "lower"

electrode being surrounded by a lower insulating element with a circular contour, said substrate being positioned in said enclosure so that its rear face is in contact with said lower electrode and with said lower insulating element, so as to define an exclusion area on the rear face, inaccessible to the plasma and the upper insulator being positioned at a distance from the front face of said SeOI substrate, so as to define an exclusion area on the front face also inaccessible to the plasma, the outer diameters of both lower and upper insulating elements, being less than the diameter of the SeOI substrate to be routed, the remainder of this substrate forming said peripheral annular area accessible to the plasma,

- depositing said layer of a protective material on said peripheral annular area, by means of a plasma formed in said enclosure,
- bringing the upper insulator closer to the front face of said SeOI substrate and performing said partial etching of the protective material,
- while maintaining the upper insulator in its position, etching a thickness of the material forming said SeOI substrate,
- moving the upper insulator away from the front face of said substrate and removing said ring of protective material,

. the routing and encapsulation steps are followed by a sacrificial oxidation step and then by a deoxidation step.

. said sacrificial oxidation and deoxidation steps are followed by a rapid thermal annealing (RTA) treatment, and then optionally by a second sacrificial oxidation and by a second deoxidation, the latter however not being indispensable since the encapsulation

is then achieved by the last rapid annealing (RTA) step.

. the method comprises a first series of steps including a rapid thermal annealing (RTA) treatment followed by sacrificial oxidation and deoxidation and in that this first series of steps precedes said steps for routing and encapsulating the substrate.

Other features and advantages of the invention will become apparent from the description which will now be made, with reference to the appended drawings, which illustrate as an indication and not as a limitation, a possible embodiment thereof.

On these drawings, in addition to the ones already described:

- Figs. 6A-6C are diagrams illustrating the different method steps according to the invention,

- Figs. 7A-7D are diagrams illustrating, as a sectional view, a portion of the substrate to be routed and of an installation allowing application of routing, during the different progression stages of the routing, respectively.

In the diagrams of Figs. 3, 6A-6C and 7A-7D, it will be noted that the respective proportions of the different illustrated layers or elements have not always been observed, certain areas having voluntarily been enlarged for explanatory purposes.

The method according to the invention is a so-called "finishing" method for a substrate of the semiconductor-on-insulator SeOI type, since it relates to steps carried out after the detachment annealing which results in the transfer of layer(s) and in the formation of this substrate comprising an insulator layer buried between two semiconducting material layers.

The method according to the invention will now be described with reference to Figs. 6A-6C.

Referring to Fig. 6A, a substrate 4 of the SeOI type may be seen which successively comprises a surface layer 41 of semiconducting material, a buried insulator layer 42 and a support 43 also made in a semiconducting material.

As this may be seen in this figure, at the end of the step for transferring layer(s), the substrate SeOI obtained 4 has defects of the aforementioned type, i.e. flakes 44, only one of which is visible in this figure, and an annular peripheral jagged edge referenced as 45.

The first step of the method according to the invention consists of carrying out routing of the peripheral annular edge of the substrate 4. This step is illustrated in Fig. 6B.

Its application methods will be described hereafter. This routing step has the effect of removing over a certain width L the edge of the surface layer 41 and the edge of the buried insulator layer 42. Preferably, this routing is conducted so as to route the substrate at a constant and controlled distance from the physical edge of the substrate.

Optionally, the routing may also be conducted until a portion of the annular periphery of the support 43 is removed over a depth P.

L is a width typically varying from 0.5 to 3 mm. L is selected to be slightly greater than the width of the crown present on the SeOI so as to remove by routing the defects of the flake or jagged edge type and to obtain a crown of constant width after routing.

P varies from 0 to a few thousands of angstroms, typically 500-1,000 Å (50 to 100 nm).

In Fig. 6B, the supporting substrate 43 has not been illustrated as routed.

The routed substrate is referenced as 4'.

The following step illustrated in Fig. 6C, consists of achieving encapsulation of the routed lateral edge 420 of the buried insulator 42. This step has the effect of causing flow of the semiconducting material forming the surface layer 41 facing this edge 420, which has the effect of protecting it and of making it inaccessible to subsequent chemical etchings, while thereby avoiding delamination phenomena.

The portion of the material 41 encapsulating the insulator 42 is referenced as 410. The routed and encapsulated substrate is referenced as 4".

The methods for applying this encapsulation step will be described hereafter.

Preferably, the encapsulation step is carried out immediately after the routing one, so as to avoid any accidental contamination of the routed substrate before the encapsulation and to at most limit the risk of alteration of the quality of the film edge obtained by routing. The encapsulation should be made before the edge looses its regularity. The film consisting of the surface layer 41 and of the buried insulator 42 is then only still slightly adhered to the receiving supporting substrate 43 and its edge notably should be reinforced in order to avoid tears or scratches.

According to an alternative embodiment, the encapsulation may also be carried out immediately after a cleaning step, itself carried out after routing.

Routing:

This routing may be carried out by various techniques and notably by mechanical grinding or an etching step.

The grinding may for example be achieved by placing the substrate 4 on a support driven into rotation, by bringing into the proximity of its edge, a polishing shoe, optionally covered with an abrasive solution ("slurry") and by applying the latter on the edge of the substrate 4 over a width L to be routed.

Reference may be made on this subject to documents US 6,797,632 and US 2007/0243694 which describe routing by grinding and/or polishing.

The routing may also be carried out by wet or dry etching.

Wet etching consists of forming a protective mask on a central portion of the front face 411 of the surface layer 41, this mask being of a diameter of less than that of the layer 41, so as to leave an unprotected annular peripheral area. The substrate is then successively exposed to specific etching solutions for the materials forming the surface layer 41 and the insulating layer 42, so as to etch and remove the unprotected edges of the substrate 4.

Dry etching consists of submitting the edge of the substrate 4 unprotected by a mask, to gas etching, for example with an isotropic or anisotropic plasma.

Reference may for example be made to document US 2009/0170285 which describes a dry etching method.

When it is desired to obtain a particularly clean routed edge, i.e. perpendicular or quasi perpendicular to the plane of the front face 411, it is possible to use the installation and the routing method which will now be described in connection with Figs. 7A-7D.

In these figures, the substrate 4 is chamfered, so that its front face 411 is broken down into a non-chamfered planar central area 411a and into

a chamfered peripheral area 411b and so that also its rear face 430 is broken down into a non-chamfered planar area 430a and a chamfered area 430b.

Its side edge is referenced as 46.

The routing is carried out inside a reactor 5 for forming plasma, as the one illustrated in Figs. 7A-7D.

This reactor comprises an enclosure 50, inside which are installed two insulating elements 53, 54 and two electrodes 51, 52, the latter being connected to an electric power supply not shown in the figures.

The substrate to be routed 4 rests on the lower electrode 52 and the lower insulating element 54, through its rear face 430.

The lower electrode 52 is surrounded by the lower insulating element 54 with a circular contour. Preferably, the electrode 52 is circular and the insulating element 54 is annular.

Moreover, the upper insulator 53 is disk-shaped and the electrode 51 which surrounds it is ring-shaped.

The upper insulating element 53 is mounted on driving means, not shown in the figures, which allow its displacement along a vertical axis perpendicular to the middle plane of the substrate 4, itself parallel to the rear face 430. It may thereby be displaced between a position illustrated in Fig. 7D, in which it is at most moved away from the substrate 4 to be routed and a position illustrated in Figs. 7B and 7C, in which it is brought closer to this substrate 4.

The gases used for forming a plasma are introduced into the inside of the enclosure 50 via ducts, for example here two in number, referenced as 55 and 56.

The volatile materials, produced during the reaction which occurs in the inside of the enclosure 50, may be discharged out of the latter by suction means and through an orifice not shown in the figures.

Voltage is applied to the electrodes 51 and 52, which has the effect of generating an electric field inside the enclosure 50 and of transforming the gases introduced into the ducts 55 and 56 into plasma.

Different parameters, such as the temperature and pressure prevailing inside the enclosure 50, the nature, the flow rate and the ratios of the gases introduced into the inside of the enclosure 50, the frequency of the plasma as well as the power applied on the terminals of the electrodes 51 and 52 have an incidence on the chemical composition of the formed plasma and on its nature, i.e. a deposition plasma or an etching plasma. These parameters will be detailed hereafter.

Preferably, the plasma formed both for deposition and for etching is isotropic. This means that the action of the plasma is preferably achieved via radicals created in the plasma, and optionally may be carried out via ions accelerated in the sheath of the plasma.

The fact that the rear face 430 of the substrate 4 is in contact with the lower electrode 52 and with the lower insulator 54, allows an exclusion area to be defined on the rear face, referenced as 540, inaccessible to the plasma since it is masked.

As this may be seen in the figures, the outer diameter of the insulator 54 exactly corresponds to the diameter of the exclusion area on the rear face 540 since the substrate 4 to be routed is directly in contact with the insulator 54.

Further, the substrate to be routed 4 is of course positioned so as to be centered relatively to the annular insulator 54.

Moreover, the upper insulator 53 also allows definition on the front face 411 of the substrate, of a so-called "front face exclusion" area 530, inaccessible to the plasma.

The diameter of the front face exclusion area 530 not only depends on the diameter of the upper insulator 53, but also on its distance from the substrate to be routed 4. Thus, the more the insulator 53 is moved away from the front face 411 of the substrate and the smaller is the diameter of the front face exclusion area 530 (see Fig. 7A), and conversely, the more it moves closer and the larger is the diameter of this area 530 (see Fig. 7B).

The annular peripheral area substrate 4 which remains accessible to the plasma, i.e. the area which extends out of the aforementioned areas 530 and 540, is referenced as 500.

The different steps of the routing method will now be described.

After the substrate to be routed 4 has been introduced into the enclosure 5, so that its rear face 430 rests against the insulating element 54 and the lower electrode 52, the parameters for forming the plasma are adjusted so as to deposit on said accessible annular area 400, a layer of a protective material 6.

Preferably, this protective material 6 is a polymer.

Still preferably, this is a polymer of the polyethylene type, obtained with a plasma formed from ethylene C_2H_4.

The upper insulator 53 is then brought closer to the front face 411 of the substrate 4, so as to

enlarge the front face exclusion area 530 and to increase the diameter thereof. It will be noted that the insulator 53 is never brought into contact with the upper face 411 of the substrate, so as to avoid damaging the latter or contaminating the latter.

In this position, illustrated in Fig. 7B, the parameters of the plasma are adapted so as to achieve partial etching of the protective material 6. This etching is partial, so that it gives the possibility of only keeping a ring 60 of protective material on the front face 411 of the substrate 4.

This partial etching is possible because of the enlargement of the front face exclusion area 530. In the position of the insulator 53 illustrated in Fig. 7A, the area where the ring 60 is found is accessible by the plasma and the protective material 6 was able to be deposited therein. On the other hand, when the insulator 53 is lowered, the portion of the protective material corresponding to the ring 60 is no longer accessible by the plasma and is therefore not etched by the latter. In other words, when the surface area of the front face exclusion area 530 increases, the latter of the accessible area 500 decreases. The reduced accessible area bears reference 500'.

The nature of the plasma for etching the protective material 6 is of course dependent on the chemical nature of this material.

As an example, for a protective material in polyethylene, etching is carried out with a plasma based on oxygen (O_2).

The following step is illustrated in Fig. 7C. While maintaining the upper insulator 53 in the position illustrated in Fig. 7B, the nature of the gases introduced into the inside the enclosure 50 is changed so as to generate a plasma capable of etching

the material of the surface layer 41 at the peripheral annular area accessible to the plasma 500'. The parameters are then modified for etching the insulator layer 42.

As an example, when the material forming the surface layer 41 is silicon, the etching plasma is a mixture of argon and SF_6 (sulfur hexafluoride) and optionally nitrogen and when the material forming the insulator 42 is oxide, the etching plasma is then a mixture of nitrogen and CHF_3 (trifluoromethane) or further a mixture of oxygen (O_2) and of tetrafluoromethane (CF_4).

As illustrated in Fig. 7C, a routed substrate 4 is obtained at its periphery not only on its front face, its rear face but also on its side.

If necessary, routing may be continued in order to etch a portion of the support 43 over a depth P.

Finally, as illustrated in Fig. 7D, the upper insulator is then moved away from the front face 41 of the substrate 4 and the parameters of the plasma are modified so as to generate an etching plasma allowing removal of the ring 60 of protective material. This etching plasma is generally the same as the one used in the etching step illustrated in Fig. 7B.

For all the steps which have just been described and which relate to the use of a deposition plasma or an etching plasma, the conventional frequency of the plasma is 13.56 MHz. The power is of the order of 100 to 500 W. The duration of application of the plasma varies between 5 and 40 seconds. The combination of the power and of the duration of the plasma notably induces an effect on the etched thickness. Finally, the pressure inside the enclosure is of the order of a few

torrs (1 torr being equal to about 10^2 Pa or more precisely 133 Pa).

Encapsulation:

This encapsulation may be achieved with a rapid thermal annealing treatment known under the acronym of "RTA" (Rapid Thermal Annealing), which may advantageously be preceded by a cleaning step.

Typically, this may be standard cleaning such as a sequence: ozone (O_3)/ RCA, the latter treatment consisting of treating the surfaces successively with:

- a first bath of a solution known under the acronym of "SC1" ("Standard Clean 1" which means "standard cleaning solution 1"), and which comprises a mixture of ammonium hydroxide (NH_4OH), of hydrogen peroxide (H_2O_2) and of deionized water,
- a second bath of a solution known under the acronym of "SC2" ("Standard Clean 2", which means a "standard cleaning solution 2"), and which comprises a mixture of hydrochloric acid (HCl), of hydrogen peroxide (H_2O_2) and of deionized water.

The RTA treatment is carried out at a high temperature for a short period.

Preferably, this heat treatment is carried out at a temperature comprised between about 1,150°C and 1,300°C, still preferably at about 1,200°C. This treatment is conducted for a duration of 15 seconds to 5 minutes, preferably for less than 3 minutes. This RTA is preferably achieved in a hydrogen and/or argon atmosphere.

The encapsulation treatment may also be carried out by epitaxy.

The encapsulation may be achieved by an RTA treatment followed by epitaxy or vice versa, these steps being achieved under the same conditions as those described earlier.

The encapsulation may also be achieved with laser annealing, ("laser anneal"), this annealing may optionally be local and limited to the edge of the routed film comprising the surface layer 41 and the insulator 42.

The method according to the invention therefore has many advantages. With it, it is possible to obtain a peripheral crown width L1 around the encapsulated portion, not only regularly all around the SeOI substrate but also in a reproducible way from one substrate to the other (see Fig. 6C).

The method according to the invention further allows a substantial reduction in the overall defectivity of the substrates made. Indeed, the routing step not only allows removal of the flakes 44 and of the jagged edges 45, but also of a large proportion of the particles present at the edge and which in the absence of such a step, would be capable of being deposited on the surface layer 41 of the SeOI during the cleaning step preceding the RTA treatment. Without this routing step, such semiconducting material particles may be displaced from the periphery towards the centre of the substrate and be definitively sealed on this substrate during the RTA treatment.

Finally, the invention finds a particular application in finishing treatments including sacrificial oxidation and deoxidation steps.

Two exemplary methods will be mentioned including the finishing steps according to the invention.

A first method comprises the following steps:

- detachment in order to carry out transfer of layer(s) and obtaining the SOI substrate,
- routing followed by an encapsulation treatment according to the method of the invention,

- first sacrificial oxidation, followed by a first deoxidation,
- RTA treatment,
- optionally a second sacrificial oxidation step followed by a second deoxidation step.

A second method is the following:

- detachment for carrying out transfer of layer(s) and obtaining the the SOI substrate,
- RTA treatment,
- a first sacrificial oxidation, followed by a first deoxidation,
- routing followed by encapsulation treatment according to the method of the invention,
- optionally a second sacrificial oxidation step followed by a second deoxidation step.

Both of these methods are particularly used for providing substrates intended for partially or fully depleted SOI applications.

CLAIMS

1. A finishing method for a substrate (4) of the semiconductor-on-insulator SeOI type comprising an insulator layer (42) buried between two layers of semiconducting material (41, 43), characterized in that it successively comprises:

- routing of the annular periphery of said substrate (4) so as to obtain a routed substrate (4'),
- encapsulation of the routed substrate (4'), so as to cover the routed side edge (420) of said buried insulator layer (42), by means of a semiconducting material (410).

2. The method according to claim 1, characterized in that the encapsulation of the routed substrate (4') is carried out immediately after routing.

3. The method according to claim 1 or 2, characterized in that the routing is carried out by grinding of the peripheral annular edge of said SeOI substrate (4).

4. The method according to claim 1 or 2, characterized in that the routing is carried out by etching of the peripheral annular edge of said SeOI substrate (4).

5. The method according to any of the preceding claims, characterized in that the encapsulation of the routed substrate (4') is carried out by submitting it to a rapid thermal annealing (RTA) treatment.

6. The method according to claim 5, characterized in that the rapid thermal annealing (RTA) treatment is conducted at a temperature comprised between 1,150°C

and 1,300°C, for a duration comprised between 15 seconds and about 5 minutes.

7. The method according to claim 5 or 6, characterized in that the rapid themal annealing (RTA) treatment is conducted under a hydrogen and/or argon atmosphere.

8. The method according to any of claims 1 to 4, characterized in that the step for encapsulating the routed substrate (4') is carried out by epitaxy.

9. The method according to any of the preceding claims, characterized in that the step for encapsulating the routed substrate (4') is carried out by rapid thermal annealing (RTA) treatment and by epitaxy.

10. The method according to any of claims 1 to 4, characterized in that the step for encapsulating the routed substrate (4') is carried out by annealing with a laser.

11. The method according to any of the preceding claims, characterized in that the routing comprises the steps of:

- depositing a layer of a protective material (6) on a peripheral annular area of said SeOI substrate (4), by means of a plasma,
- achieving partial etching of said protective material (6) by means of a plasma, so as to keep a ring of protective material (60) on the front face (411) of said SeOI substrate (4), this ring (60) extending at a distance from the side edge (46) of said substrate, and to thereby delimit a reduced peripheral annular area (500') of said substrate accessible to a plasma,

- generating a partial etching plasma, localized at said reduced peripheral annular area of the SeOI substrate (4), so as to etch the material present in this area (500') over a certain thickness,
- removing said ring of protective material (6) by means of a plasma.

12. The method according to claim 11, characterized in that the routing is carried out in an enclosure (50) for forming an isotropic plasma.

13. The method according to claim 12, characterized in that the routing is carried out by steps consisting of:
- introducing said SeOI substrate (4) inside an enclosure (50) for forming an isotropic plasma, equipped with an upper disk-shaped insulating element (53) and with two electrodes (51, 52), one of them (52), a so-called lower electrode being surrounded by a lower insulating element (54) with a circular contour, said substrate (4) being positioned in said enclosure (5) so that its rear face (430) is in contact with said lower electrode (52) and with said lower insulating element (54), so as to define an exclusion area (540)on the rear face, inaccessible to the plasma and the upper insulator (53) being positioned at a distance from the front face (411) of said SeOI substrate (4), so as to define an exclusion area (530)on the front face also inaccessible to the plasma, the outer diameters of both lower (54) and upper (53) insulating elements being less than the diameter of the SeOI substrate (4) to be routed, the remainder of this substrate forming said peripheral annular area (500) accessible to the plasma,

- depositing said layer (6) of a protective material on said peripheral annular area (500), by means of a plasma formed in said enclosure (50),
- bringing the upper insulator (53) closer to the front face (411) of said SeOI substrate and performing said partial etching of the protective material (6),
- while maintaining the upper insulator (53) in its position, etching a thickness of the material forming said SeOI substrate (4),
- moving the upper insulator (53) away from the front face (411) of said substrate and removing said ring (60)of protective material.

14. The method according to any of the preceding claims, characterized in that the routing and encapsulation steps are followed by a sacrificial oxidation step and then by a deoxidation step.

15. The method according to claim 14, characterized in that said sacrificial oxidation and deoxidation steps are followed by a rapid thermal annealing (RTA) treatment, and then optionally by a second sacrificial oxidation and by a second deoxidation.

16. The method according to any of the preceding claims, characterized in that it comprises a first series of steps including a rapid thermal annealing (RTA) treatment followed by sacrificial oxidation and deoxidation and in that this first series of steps precedes said steps for routing and encapsulating the substrate.