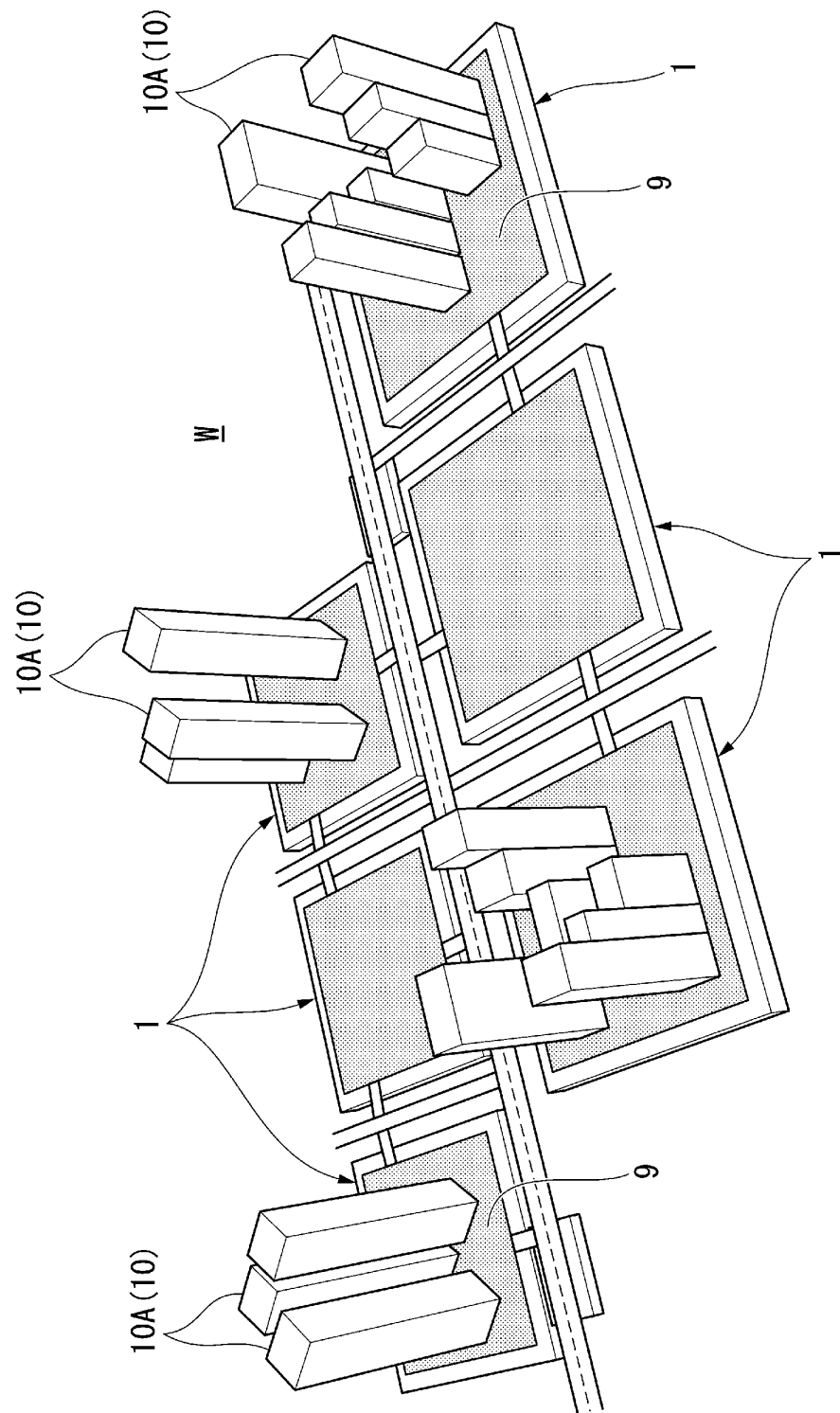


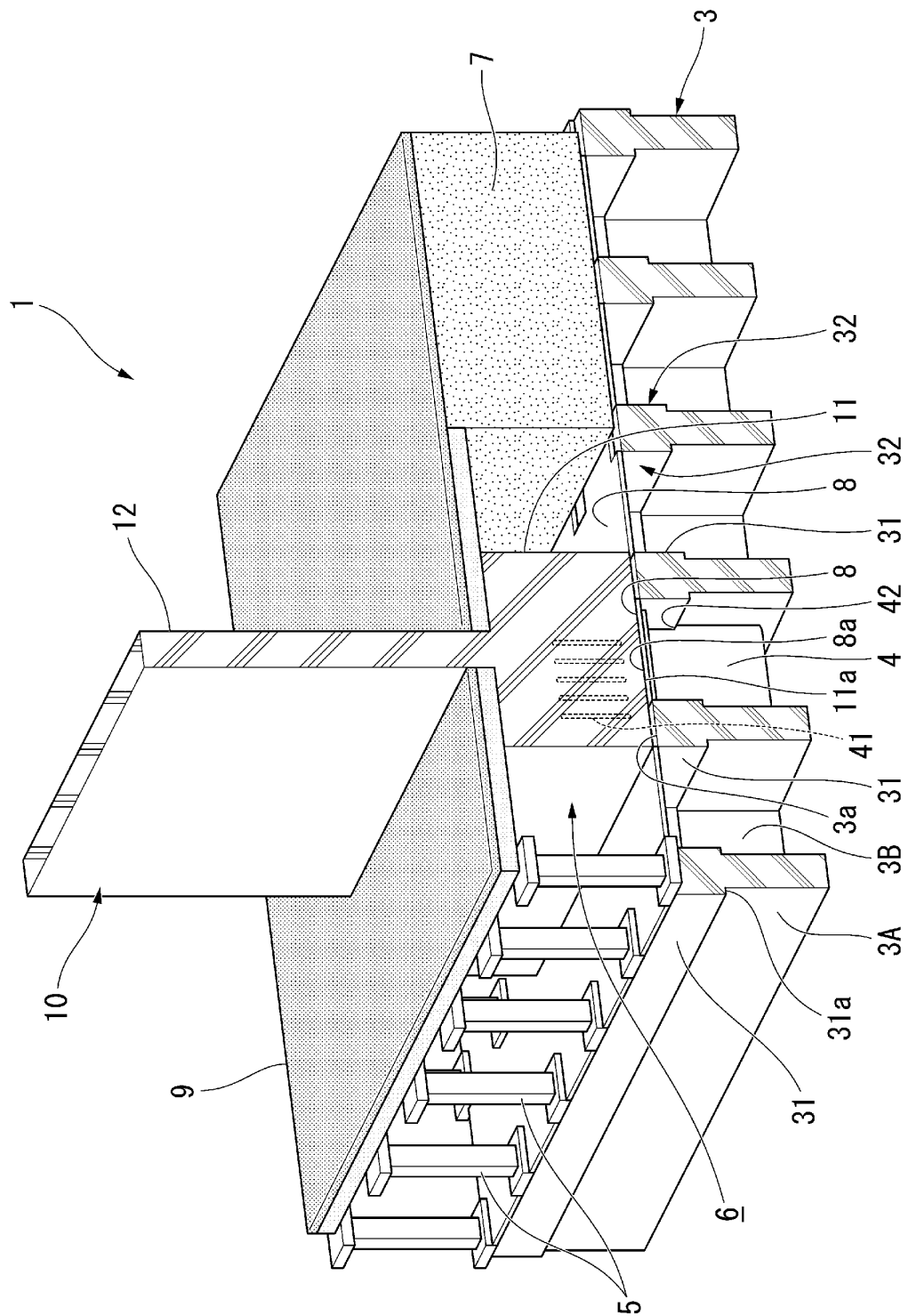
[図1]



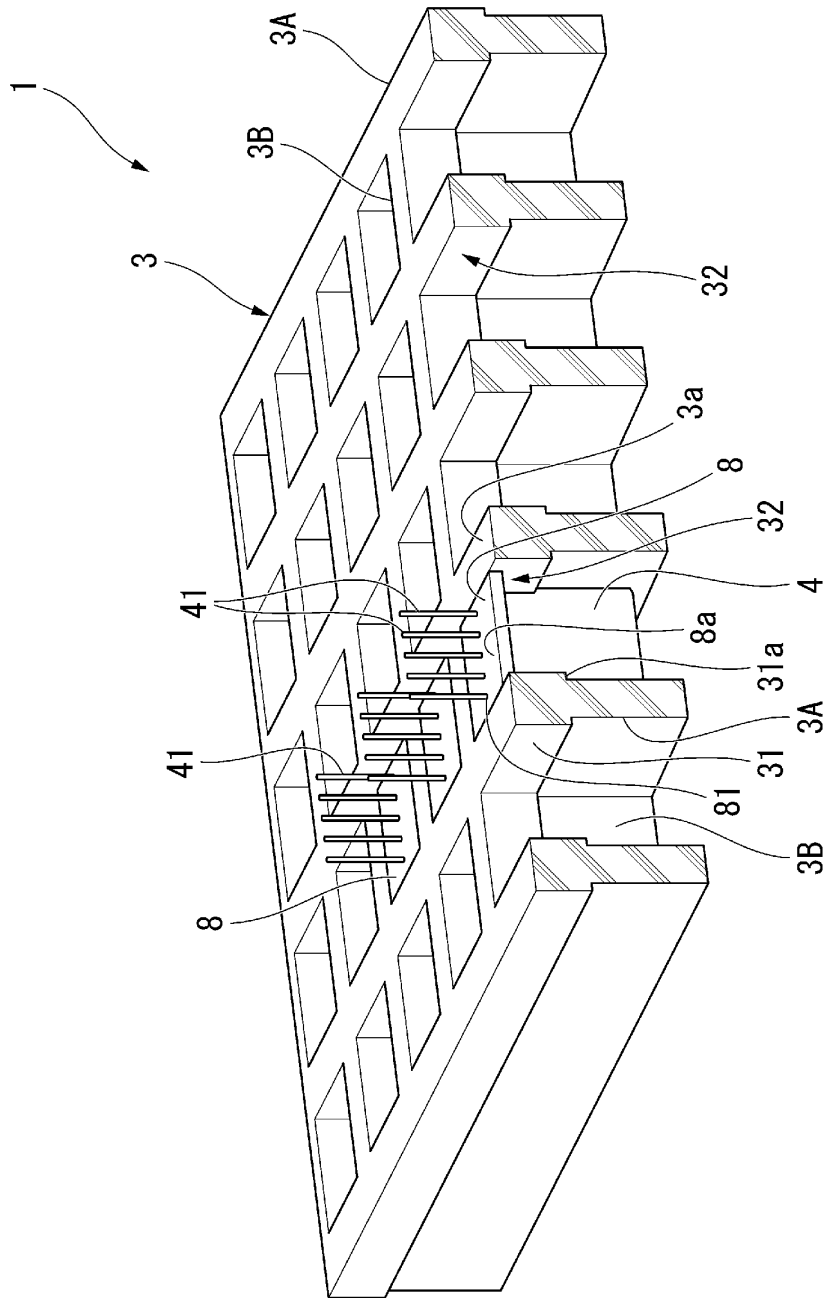


A cross-sectional view of a semiconductor device 1. The device features a substrate 2 with a top surface 2a and a side surface 2b. A layer 3 is formed on the top surface 2a. A series of vertical pillars 5 are formed in the layer 3, with a gap 6 between them. A horizontal layer 8 is formed on top of the pillars 5. A layer 9 is formed on top of the layer 8. A layer 14 is formed on the side surface 2b of the substrate 2. A layer 32 is formed on top of the layer 14.

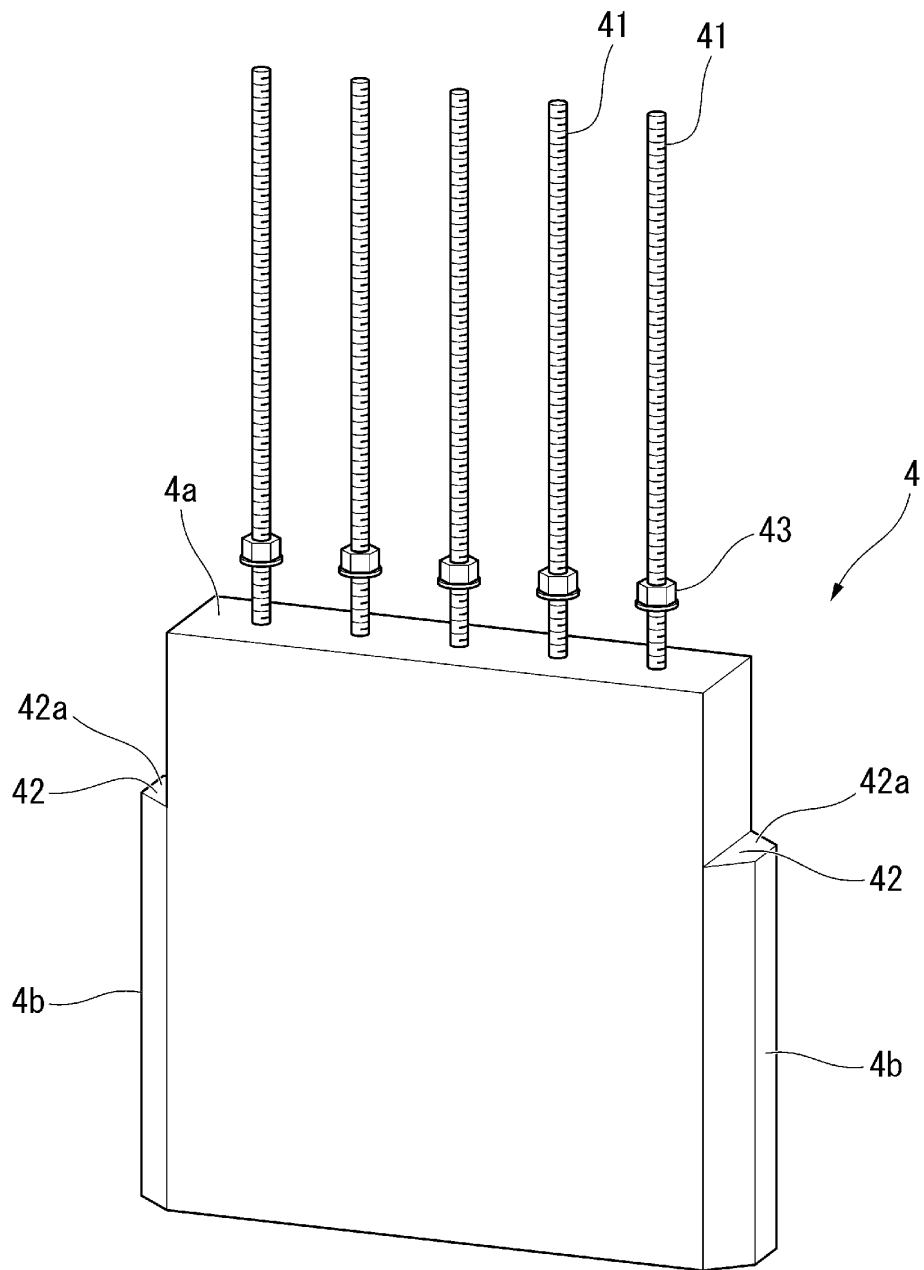
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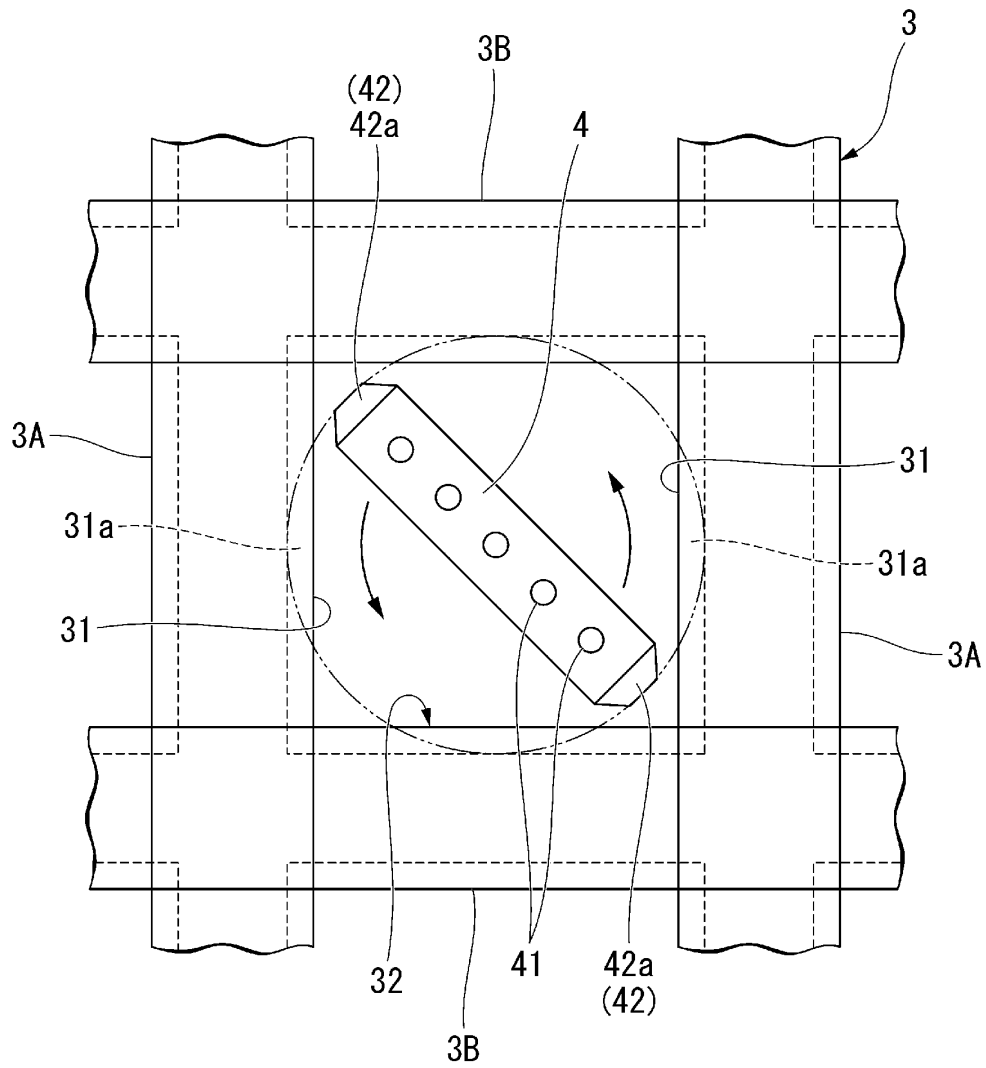


[図5]

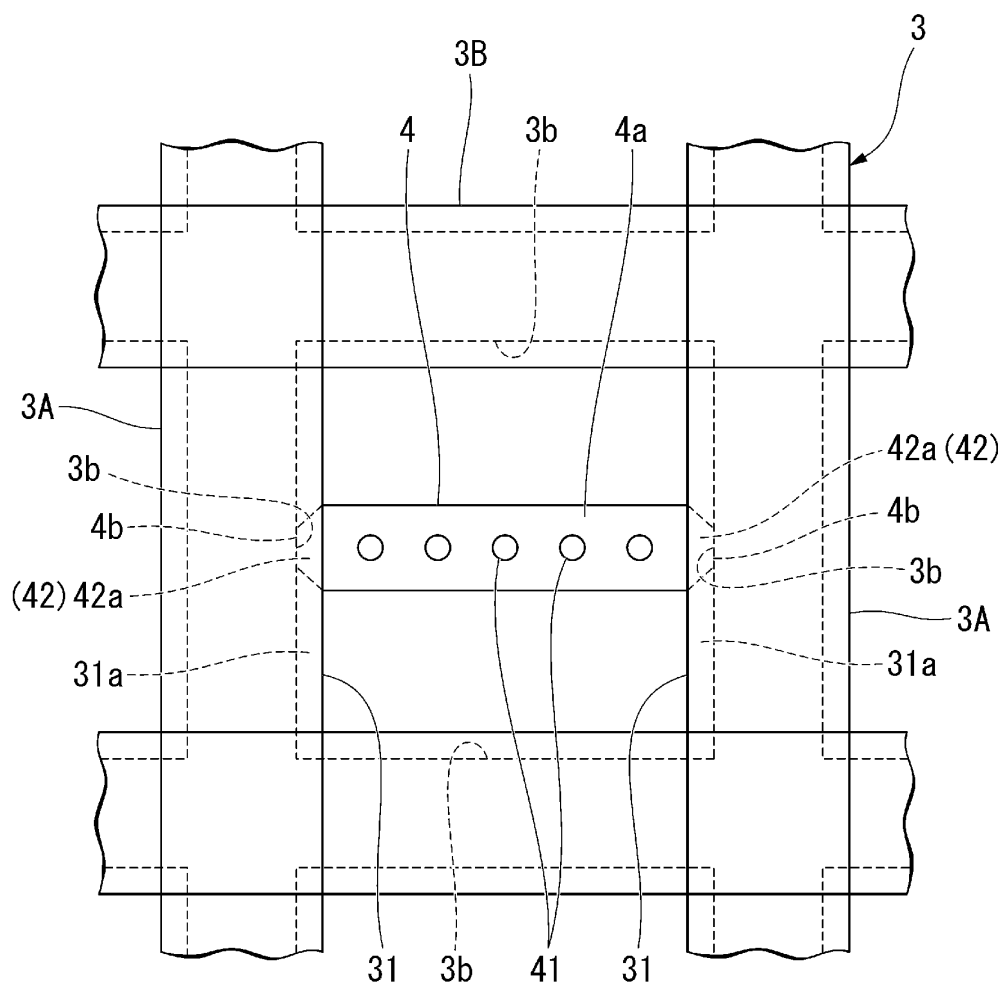


[図6]

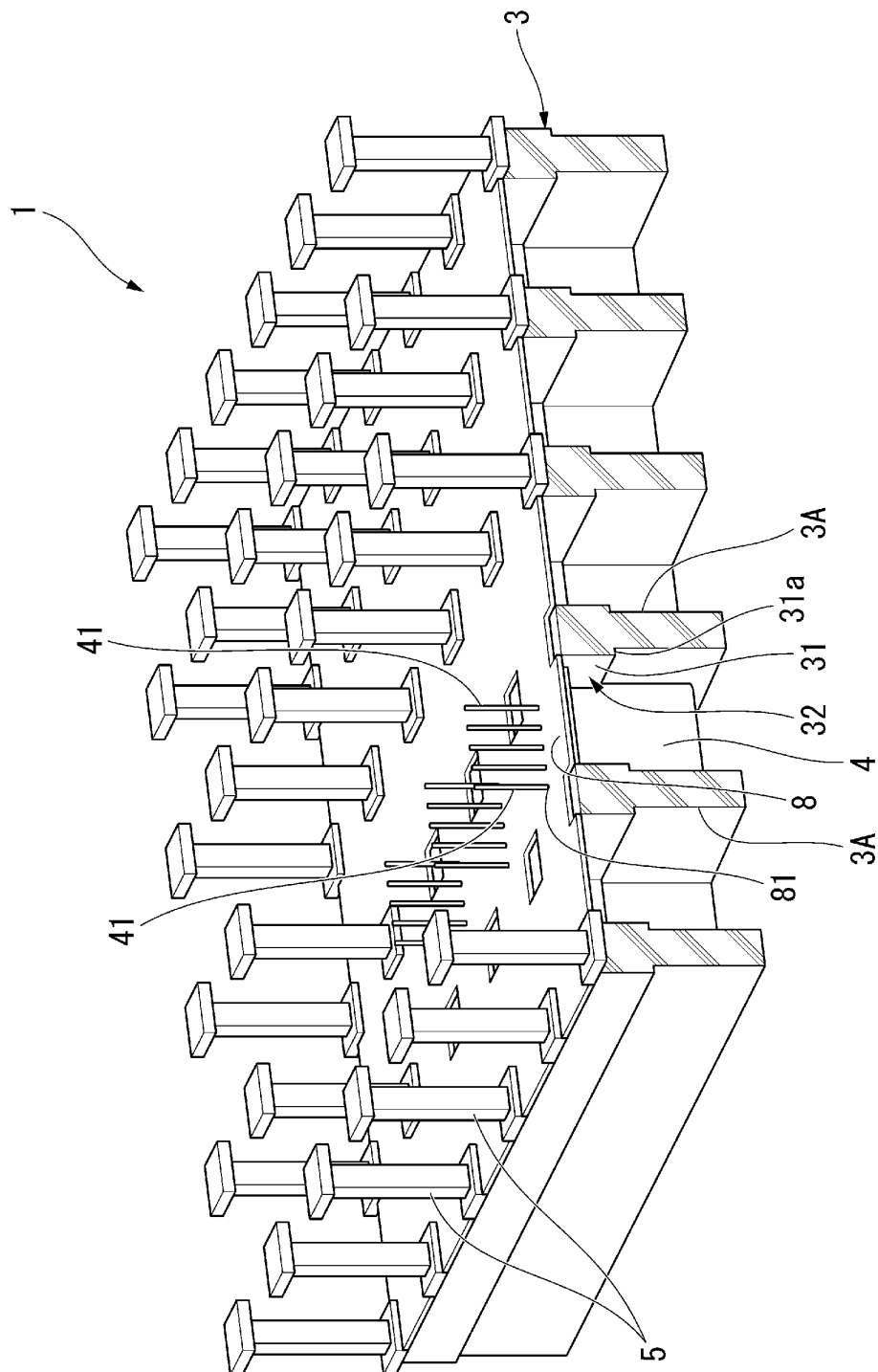




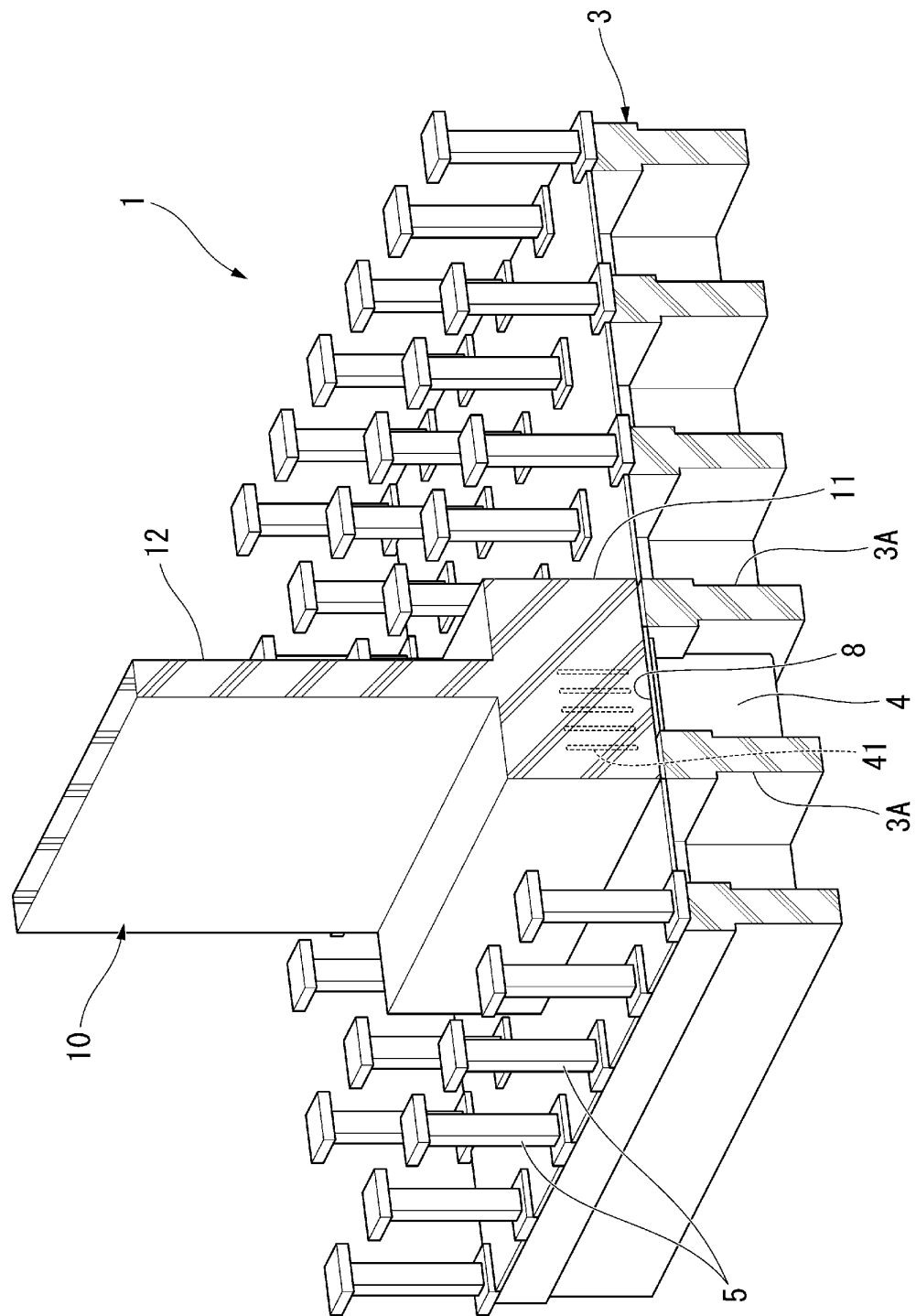
[図8]



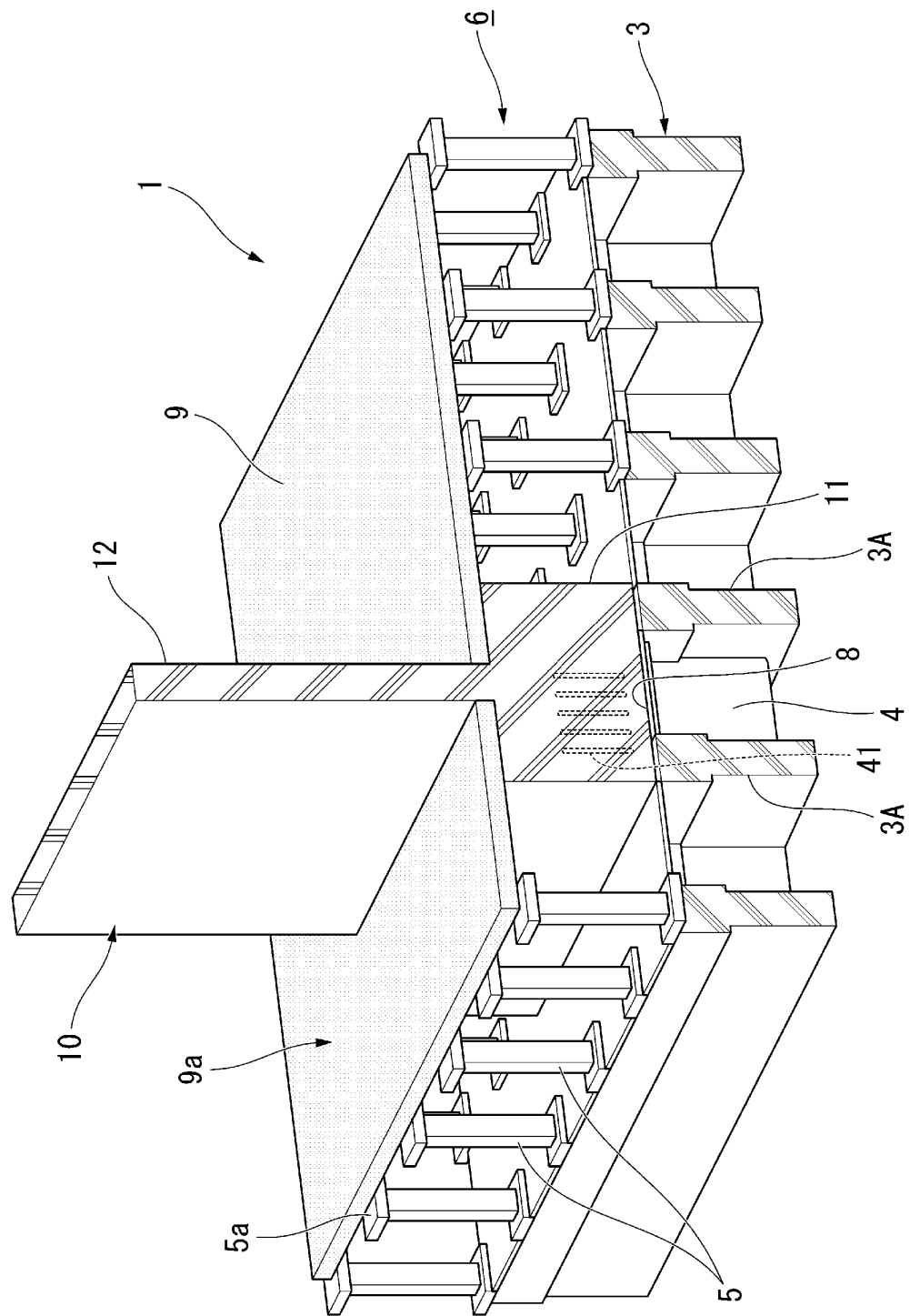
[図9]



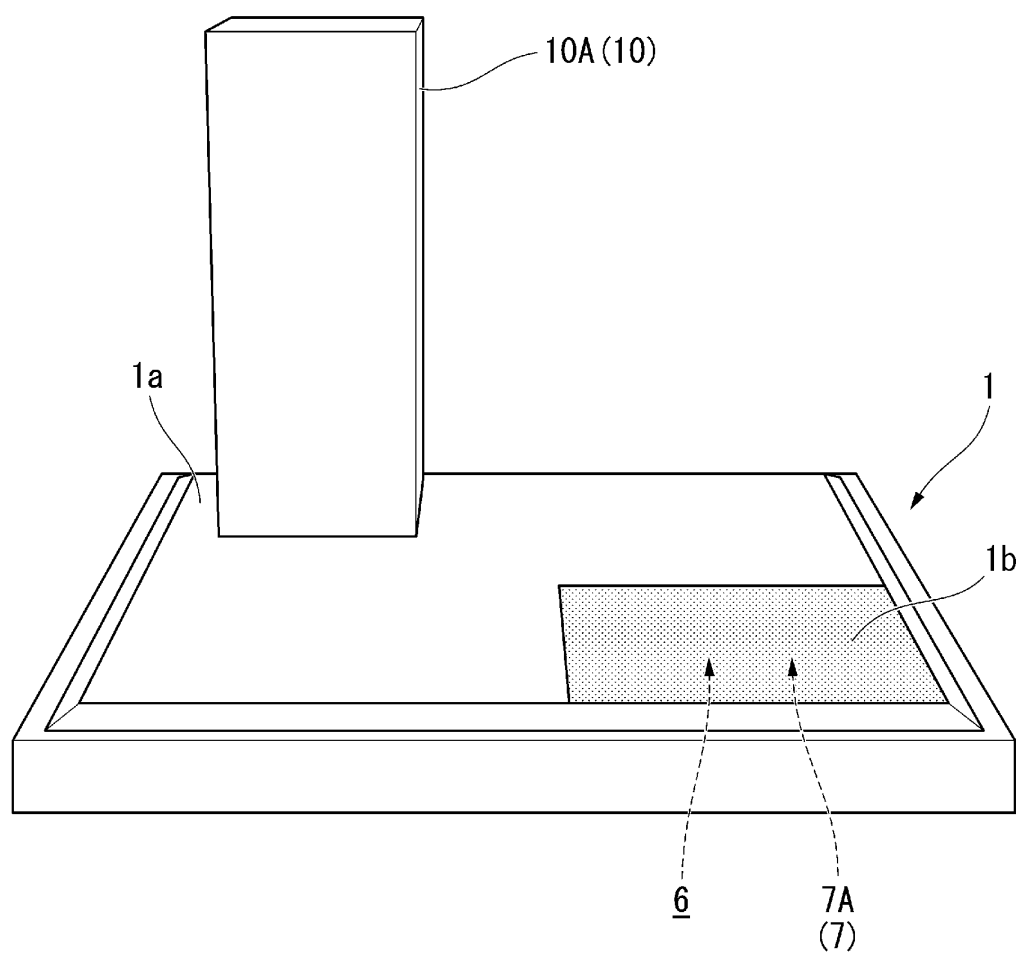
[図10]



[図11]



[図12]



[図13]

