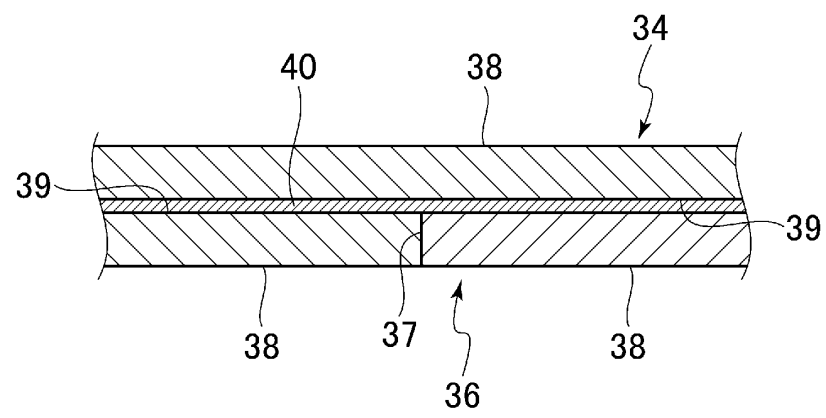
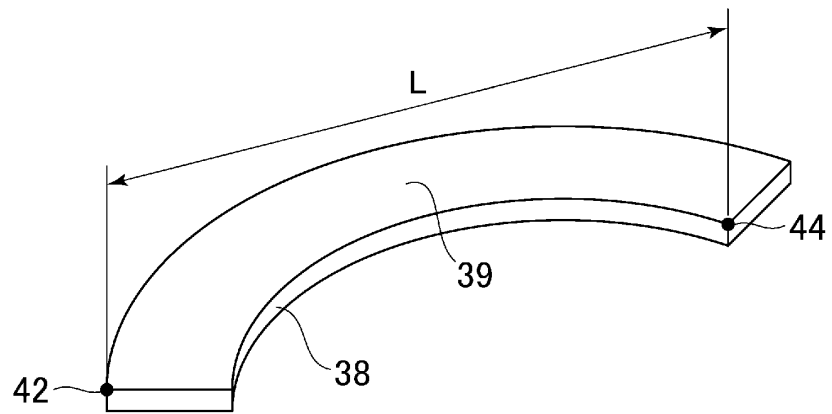


A cross-sectional view of a semiconductor device 10. The device features a substrate 12 with a top layer 14. A gate stack 15 is formed on the top layer 14, with a gate electrode 22. A source/drain region 16 is formed in the substrate 12, with a contact plug 18. A passivation layer 19 is formed over the gate stack 15 and the source/drain region 16. A contact pad 20 is formed on the passivation layer 19, with a contact plug 24. A metal line 26 is formed on the contact pad 20, with a contact plug 28. A ground symbol is connected to the metal line 26. A dashed line 30 indicates a cross-section line.

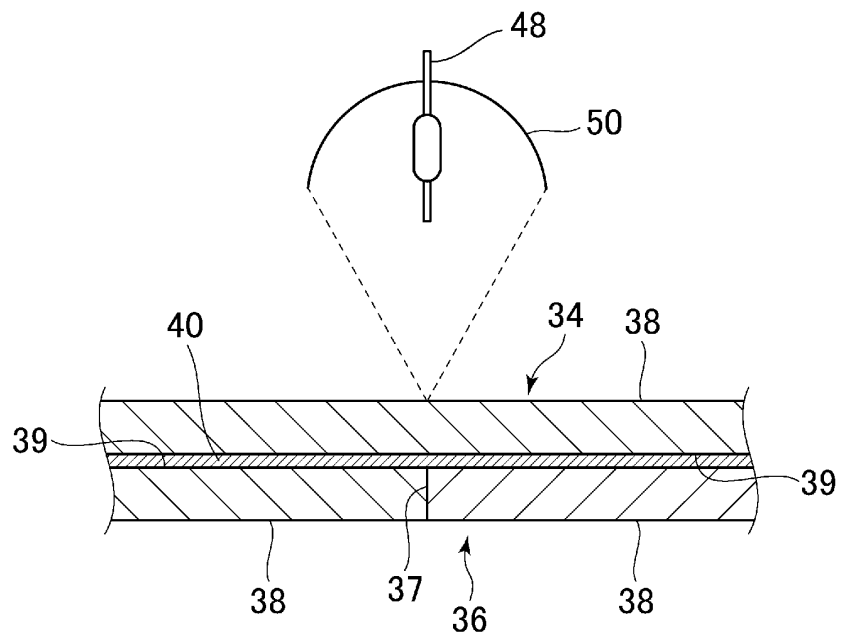
[図3]



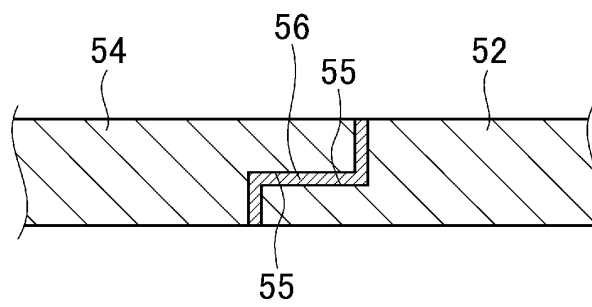
[図4]



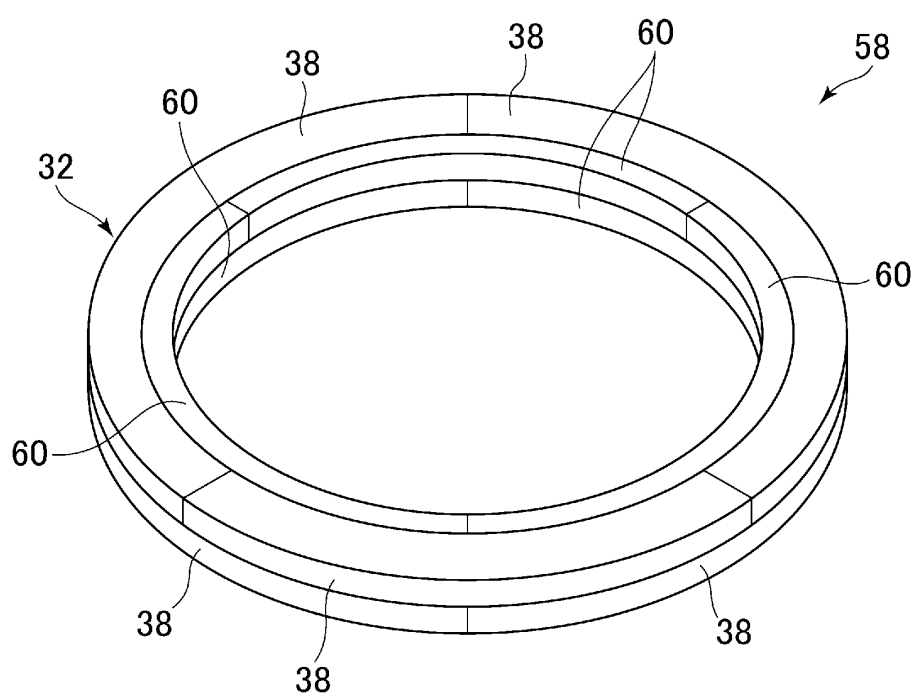
[図5]



[図6]



[図7]



[図8]

