NEGATIVE CAPACITANCE TOPOLOGICAL QUANTUM FIELD-EFFECT TRANSISTOR

Field

[0001] The invention relates to an electronic structure that comprises a topological insulator layer located adjacent to at least one layer of a negative capacitance material (such as a ferroelectric material). These structures have particular application as low-voltage field effect transistors.

Background

[0002] In transistors, a large fraction of power dissipation occurs due to irreversible charging and discharging of the gate capacitor to turn conduction on and off. Its efficiency is characterized by the sub-threshold swing, such that a transistor with a small sub-threshold swing transitions rapidly between its on (high current) and off (low current) states. The sub-threshold swing is the fundamental critical parameter determining the operation of a transistor in low-power applications such as switches.

[0003] In a conventional field-effect transistor, a voltage V_g applied to the gate raises an energy barrier E_g in the channel which impedes conduction, realizing a switch. The effective sub-threshold swing S^* is given by $S^*=e[dE_g/dV_g]^{-1}$. and it is well-known that thermal activation of carriers in the channel forces $S^* \geq 1$, often termed “Boltzmann’s tyranny”. In a topological quantum field-effect transistor, a voltage difference V_g between two gates produces an electric field, and induces a sublattice potential difference λ_v which opens a gap E_g, which acts as a barrier to conduction. The effective sub-threshold swing S^* for a topological transistor is given by $S^*=e[dE_g/d\lambda_v]^{-1}$, and $\lambda_v \leq V_g$, $S^* = 1$ corresponds to Boltzmann’s limit. In the simplest models the gap equates to the potential difference established by the gates λ_v, and one expects $S^* \geq 1$. However, Rashba spin-orbit coupling can result in $S^* < 1$ in a topological quantum field-effect transistor, making this device promising for low-voltage applications. Potential shortcomings, however, are that λ_v may be substantially less than V_g dues to screening in the topological channel material, and the strength of Rashba spin-orbit coupling is limited.

[0004] It is therefore desirable to further reduce the subthreshold swing in topological transistor devices to reduce power dissipation and improve the efficiency of these devices.

[0005] It is an object of the invention to address one or more shortcomings of the prior art and/or provide a useful alternative.

[0006] Reference to any prior art in the specification is not an acknowledgment or suggestion that this prior art forms part of the common general knowledge in any jurisdiction or that this prior art could reasonably be expected to be understood, regarded as relevant, and/or combined with other pieces of prior art by a skilled person in the art.

Summary of Invention

[0007] In a first aspect of the invention there is provided a structure comprising: a top gate electrode and a bottom gate electrode, a channel layer formed from a channel material with a band gap modulable by electric field, the channel layer being electrically insulated from the top gate electrode and the bottom gate electrode and being located adjacent to at least one layer of a negative capacitance material.

[0008] In an embodiment, the combined capacitance between the top and bottom gate electrodes is greater than 0. The purpose of balancing the negative capacitance of the negative capacitance material and the positive capacitance of the channel material is to get a net positive capacitance. The net positive capacitance ensures that there is no spontaneous and hysteretic polarization of the negative capacitance material which is undesirable, particularly in transistors.

[0009] In a second aspect of the invention there is provided a structure comprising:

a top gate electrode and a bottom gate electrode,

a planar channel layer located between the top gate electrode and the bottom gate electrode, the planar channel layer being separated from the top gate electrode by a first insulating layer and separated from the bottom gate electrode by a second insulating layer;

wherein the planar channel layer is formed from a channel material with a band gap modulable by electric field;

wherein at least one of the first insulating layer and the second insulating layer are formed from a negative capacitance material.

[0010] In an embodiment of the first or second aspects, the top gate electrode and the bottom gate electrode are operable to apply an electric field across the channel layer.

[0011] In an embodiment of the first or second aspects, the top gate electrode and the bottom gate electrode are operable independently of one another.

[0012] In an embodiment, the structure is a layered structure comprising or consisting of the following sequential layered arrangement: the first insulating layer, the planar channel layer, and the second insulating layer; wherein the top gate electrode is in electrical contact with the first insulating layer and the bottom gate electrode is in electrical contact with the second insulating layer.

[0013] In an embodiment, both of the first insulating layer and the second insulating layers are formed from the ferroelectric material. The first and second insulating layers may be formed from the same ferroelectric material or different ferroelectric materials. However, it is preferred that the first and second insulating layers are formed from the same ferroelectric material.

[0014] In an embodiment of the first and second aspects, the negative capacitance material is a ferroelectric material. Preferably, the ferroelectric material is selected from the group consisting of: $Hf_{0.5}Zr_{0.5}O_2$, La-doped HfO_2, $BiFeO_3$, $BaTiO_3$, $PbTiO_3$, $Pb[Zr_xTi_{1-x}]O_3$, and In_2Se_3.

[0015] In an embodiment, the negative capacitance material exhibits negative capacitance and wherein the channel material exhibits positive capacitance, and the combined capacitance of the channel layer, the first insulating layer, and second insulating layer is greater than 0. As discussed above, the net positive capacitance ensures that there is no spontaneous and hysteretic polarization of the ferroelectric which is undesirable, particularly in transistors. In more detail, the electric field-polarization *E*-*P* relationship for the ferroelectric layers may be expressed as $E = 2\alpha_{FE}P + 4\beta_{FE}P^3 + O(P^5)$, where α_{FE} and β_{FE} are parameters, and $O(P^5)$ indicates additional terms in powers of *P* greater than or equal to 5. The condition $\alpha_{FE} < 0$ indicates that the layer has a negative capacitance. Then the total thickness of the ferroelectric layers t_{FE} should be chosen to be as small as practicable but larger than $(2|\alpha_{FE}|C_{TI})^{-1}$, where C_{TI} is the capacitance per area of the channel layer.

[0016] In an embodiment, the first insulating layer is adjacent to the channel layer. Preferably, the first insulating layer has a first planar side adjacent to the channel layer, and an opposite facing second planar side adjacent to the top gate electrode.

[0017] In an embodiment, the second insulating layer is adjacent to the channel layer. Preferably, the second insulating layer has a first planar side adjacent to the channel layer, and an opposite facing second planar side adjacent to the top gate electrode.

[0018] In an embodiment, the first insulating layer and the second insulating layer are each in physical contact with the planar channel layer, the first insulating layer being arranged on a first side of the planar channel layer and the second insulating layer being arranged on a second side of the planar channel layer.

[0019] In an embodiment of the first and second aspects, the structure further comprises a source electrode in electrical contact with the planar channel layer, and a drain electrode spaced apart from the source electrode and in electrical contact with the planar channel layer.

[0020] In one form of the above embodiment, the source electrode is in electrical contact with the planar channel layer via a doped semiconductor material, and/or the drain electrode is in electrical contact with the planar channel layer via a doped semiconductor material.

[0021] In one form of the above embodiment, the source electrode is formed from a doped semiconductor material and/or the drain electrode is formed from a doped semiconductor material.

[0022] In an embodiment of the first and second aspects, the top gate electrode and/or the bottom gate electrode are formed from a metal.

[0023] In an embodiment of the first and second aspects, the top gate electrode and the bottom gate electrode are configured to apply an electric field across the channel layer in a direction perpendicular to a plane of the channel layer.

[0024] In an embodiment of the first and second aspects, the channel material is selected from the group consisting of: few-layer graphene (preferably bilayer or ABC-stacked trilayer graphene), a two-dimensional semiconductor (preferably monolayer or bilayer blue phosphorene

or black phosphorene), a topological material (such as a two-dimensional topological material, where “two-dimensional topological material” refers to the topological material being electronically two-dimensional).

[0025] In one form of the above embodiment where the channel material is a topological material, the topological material is in the form of a thin film with a thickness of two unit cells or less.

[0026] In one form of the above embodiment where the channel material is a topological material, the topological material exhibits a topological phase transition between a trivial state and a non-trivial state at a critical electric field strength.

[0027] In one form of the above embodiment where the channel material is a topological material, the topological material has a staggered honeycomb lattice structure. Preferably, lattice atoms of the staggered honeycomb lattice structure comprise one or more atoms selected from the group consisting of: As, Sb, Bi. Preferably, the staggered honeycomb lattice is of the form X, XY, or XYZ, where X is selected from the group consisting of As, Sb, Bi, and Y and Z are each independently selected from the group consisting of H, Cl, Br, or F.

[0028] In one form of the above embodiment where the channel material is a topological material, the topological material is a topological Dirac semimetal. Preferably, the topological Dirac semimetal is selected from the group consisting of: a material of the form A_3Bi where A is an alkali metal, Cd_3As_2.

[0029] In one form of the above embodiment where the channel material is a topological material, the topological material is a topological insulator. Preferably, the topological insulator is selected from the group consisting of: a material of the form A_3Bi where A is an alkali metal, HgTe, Bi_2Se_3.

[0030] In an embodiment of the first and second aspects, the channel layer is in the form of a thin film having a thickness of less than 10 nm.

[0031] In an embodiment of the first and second aspects, the structure is a field effect transistor or a component thereof.

[0032] In a third aspect of the invention, there is provided a method of operating a structure according to the first aspect of the invention, the second aspect of the invention, and/or embodiments thereof, and/or forms thereof, the method comprising:

applying or modulating a gate voltage to the top gate electrode and/or the bottom gate electrode to generate or vary an electric field across the channel layer in a direction perpendicular to a plane of the channel layer to alter the bandgap of the channel material in the channel layer.

[0033] In an embodiment, altering the bandgap of the channel layer further comprises switching the channel material between a trivial state and a non-trivial or topological state.

[0034] In a fourth aspect of the invention, there is provided use of a structure according to the first aspect of the invention, the second aspect of the invention, and/or embodiments thereof, and/or forms thereof in an electrical device.

[0035] In a fifth aspect of the invention, there is provided an electrical device comprising the structure according to the first aspect of the invention, the second aspect of the invention, and/or embodiments thereof, and/or forms thereof.

[0036] As used herein, except where the context requires otherwise, the term "comprise" and variations of the term, such as "comprising", "comprises" and "comprised", are not intended to exclude further additives, components, integers or steps.

[0037] Further aspects of the present invention and further embodiments of the aspects described in the preceding paragraphs will become apparent from the following description, given by way of example and with reference to the accompanying drawings.

Brief Description of Drawings

[0038] **Figure 1:** Schematic of negative capacitance topological quantum field-effect transistor. (a) Structure of the device. (b) Electrostatic potential energy as a function of distance across the device in “on” ($V_b = V_t = 0$) and “off” ($V_b > 0$, $V_t < 0$) states.

[0039] **Figure 2:** Band diagrams in “on” (topological insulator, upper diagram) and “off” (conventional insulator, lower diagram) states. The conducting helical edge states of the topological insulator are shown in the upper diagram.

[0040] **Figure 3:** Schematic band diagrams of the unipolar NC-TQFET as a function of gate voltage applied to a single gate V_g.

[0041] **Figure 4:** Bandgap as a function of gate voltage for a bilayer graphene (BLG)-ferroelectric transistor ($S^* = 1$), and a NC-TQFET with similar properties modelled on bismuthene with strong spin-orbit coupling ($S^* = 0.568$). The modeling results assuming the experimentally measured electric-field-dependent bandgap values for BLG from optical spectroscopy and electronic transport are also shown, along with a tight-binding calculation. The remanent polarization $P_r = 27.5$ μC/cm^2 corresponds to La-doped HfO_2, and $P_r = 130$ μC/cm^2 corresponds to tetragonal-like $BiFeO_3$.

Description of Embodiments

[0042] The invention broadly relates to a structure comprising: a top gate electrode and a bottom gate electrode, a channel layer formed from a channel material with a band gap modulable by electric field (such as a topological material), the channel layer being electrically insulated from the top gate electrode and the bottom gate electrode and being located adjacent to at least one layer of a negative capacitance material.

[0043] The inventors have found that this structure can be used to form a topological quantum field effect transistor (TQFET) with reduced sub-threshold swing as compared with a similar transistor without the negative capacitance material.

[0044] In particular, TQFETs are electric-field effect transistors, where the barrier to conduction is created through an electric field, rather than raising an existing potential barrier in the channel as per conventional metal–oxide–semiconductor field-effect transistors (MOSFET). Thus, a TQFET can take full advantage of electric field amplification by negative capacitance, whereas this is not possible with a conventional MOSFET since the electric field is zero in the channel in the subthreshold region.

[0045] In more detail, a conventional MOSFET has a capacitance between channel and gate which is large compared to other parasitic capacitances to the channel. In the subthreshold regime, the capacitance between channel and gate is large compared to the quantum capacitance of the channel. Under these conditions, when a gate voltage is applied, i.e. an electrochemical potential difference between gate and channel, this raises the chemical potential of the channel by the same amount, while hardly changing the electrostatic potential of the channel (the electrochemical potential difference is the sum of these two). Thus, the electrostatic potential difference between gate and channel is minimal, and there is very little electric field induced by the gate voltage. Thus, in a conventional MOSFET, because the electric field is near zero in the subthreshold regime, the device cannot benefit from amplification of the electric field through the use of a negative capacitance in series with a positive capacitance.

[0046] In contrast, in a TQFET, electric field is used to modify the bandgap of a channel material. In the subthreshold regime, the increased bandgap will act as an increased activation barrier to electron flow. This is completely different to a MOSFET: rather than using the chemical potential change to create a barrier in a semiconductor with a fixed bandgap, the electric field changes the bandgap in a channel with a fixed chemical potential.

[0047] The inventors have found that TQFET devices can benefit from amplification of the electric field through the use of a negative capacitance in series with a positive capacitance. This can be accomplished by nearly balancing the positive capacitance of the channel itself with the negative capacitance of a ferroelectric to produce a net positive capacitance (noting that the net positive capacitance ensures that there is no spontaneous and hysteretic polarization of the negative capacitance material). The electric field amplification becomes very large when this balance is near perfect. Advantageously, this amplification of the electric field means that the change in bandgap will be larger for a given change in gate voltage, and thus the subthreshold swing will be smaller.

[0048] The invention will be generally described below in relation to a preferred embodiment thereof in the form of a negative capacitance topological quantum field effect transistor (NC-TQFET).

[0049] **Figure 1a** is an illustration of an NC-TQFET according to one embodiment of the invention. The NC-TQFET 100 includes independent top 102 and bottom gates 104, a channel

formed from a 2D layer of a topological insulator (TI) 106 sandwiched between ferroelectric layers 108 and 110, and source electrode 112 and drain electrode 114 in electrical contact with channel 106.

[0050] The inventors have found that the combined structure of ferroelectric (negative capacitance) and 2D TI (positive capacitance) amplifies the electric field in the 2D TI layer as illustrated in **Figure 1b**. **Figure 1b** shows the electrostatic potential energy as a function of distance across the device in "on" state where there is zero voltage applied to bottom gate 104 and top gate 102 (e.g. $V_b = V_t = 0$), and "off" state where the voltage applied to bottom gate 104 is greater than zero and the voltage applied to top gate 102 is less than zero (e.g. $V_b>0$, $V_t<0$).

[0051] **Figure 2** shows band diagrams for the TI in "on" (topological insulator, upper diagram) and "off" (conventional insulator, lower diagram) states. With reference to **Figure 2**, the NC-TQFET is in the "on" state when the two top gate voltages $V_b = V_t = 0$; the potential across the ferroelectric/2D TI/ferroelectric structure is constant, the electric field in the 2D TI is zero, and the 2D TI is in a topological state. Applying gate voltages $V_b > 0$, $V_t < 0$ places the NC-TQFET in the "off" state, amplifying the electric field in the 2D TI, and opening a conventional bandgap and producing the potential profile shown in the "off" state in the lower diagram of **Figure 2**.

[0052] The NC-TQFET described above is ambipolar, turned off by either $V_b > 0$, $V_t < 0$ or $V_b < 0$, $V_t > 0$. Ideally an FET device should operate with a single gate as a unipolar transistor. This situation is realized by grounding one gate and applying a gate voltage to the other. Furthermore, if the NC-TQFET channel is connected to semiconducting source/drain leads, unipolar conduction results. **Figure 3** illustrates schematic band diagrams of the unipolar NC-TQFET as a function of gate voltage applied to a single gate V_g. At $V_g = 0$ the electric field is zero and the device is "on". At $V_g < 0$ the electric field is non-zero, opening a bandgap, and the net effect of the two gates is to shift the overall potential by and amount $V_g/2$. This allows a bandgap eV/S* to be opened at a gate voltage V.

[0053] To estimate the electric field amplification in the device illustrated in **Figure 1a**, the electric field-polarization *E-P* relationship for the ferroelectric layer can be approximated as $E = 2\alpha_{FE}P + 4\beta_{FE}P^3$ where $\alpha_{FE} < 0$ and $\beta_{FE}>0$ are parameters that characterize the ferroelectric. A negative value of α indicates a bistable P(E) relationship i.e. ferroelectricity. The TI layer has $E = 2\alpha_{TI}P$ with $\alpha_{TI} = +1/(2\varepsilon)$ corresponding to a linear dielectric. A relationship between the gate

voltage applied across the FE/TI/FE stack, V_g, and the surface potential difference across the TI, ψ_s:

$$V_g = (1 + a_1)\,\psi_s + a_2\psi_s^3.$$

where $a_1 = \alpha_{FE}/\alpha_{TI}$ and $a_2 = (4\beta_{FE}/\alpha_{TI}^3)t_{FE}^2$ where t_{FE} is the ferroelectric total thickness (twice the thickness of top and bottom layer). The maximum electric field amplification is when $\alpha_{FE}/\alpha_{TI} = -1$ or $t_{FE} = (2|\alpha_{FE}|C_{TI})^{-1}$. Then $V_g = ((2\beta_{FE}\, C_{TI}^2)/(|\alpha_{FE}|))*\psi_s^3 = ((C_{TI}^2)/(Pr^2))*\psi_s^3$ where $P_r = sqrt(-\alpha/(2\beta))$ is the remanent polarization.

[0054] Modelling was conducted considering bilayer graphene (BLG) as the channel material since this BLG has an experimentally characterized electric-field-dependent bandgap. However, the skilled person will appreciate that the results of this modelling are applicable to a range of topological insulator materials. For the ferroelectric negative capacitance material, La-doped HfO_2 was selected for which an assumed value of $P_r = 27.5$ μC/cm^2 was used. As above, the skilled addressee will appreciate that a range of other ferroelectric materials could be used, and particularly those based on HfO_2 / ZrO_2.

[0055] For a material with negligible spin-orbit coupling such as bilayer graphene, $S^* = 1$. The electric field is reduced by dielectric screening in the BLG layer by a dielectric constant κ. Furthermore, the separation of the atoms in the sublattice t_v is smaller than the van der Waals thickness of the layer t_{TI}, which further reduces the sublattice potential difference by an amount t_v/t_{TI}, such that $\lambda_v = (t_v/t_{TI}\kappa)\psi_s$, and $dE_g/d\psi_s$. For BLG, $t_v/t_{TI} = 0.5$, $\kappa = 3.6$, $S^* = 1$ predicts $dE_g/d\psi_s = 0.139$ which is very close to experimentally measured values from optical spectroscopy and electronic transport. The BLG capacitance $C_s = 0.048$ F/m^2 (assuming $\kappa = 3.6$, $t_{TI} = 6.68$ A) allows $E_g(V_g)$ to be calculated for the ferroelectric/BLG/ferroelectric structure (see the solid lower curve in **Figure 4**).

[0056] Certain materials, such as honeycomb Xene lattices of heavy atoms, experience a strong Rashba spin-orbit interaction due to the gate electric field. As a result, S^* can be less than 1. The inventors have found $S^* < 0.75$ in existing materials and estimate S^* as low as 0.57 in functionalized Bi (see **Table 1** below).

Table 1: Strength of atomic spin orbit interaction (SOI) ξ, Slater-Koster parameter $Vsp\sigma$ and sub-threshold swing S^* for TQFET based on group-IV and V Xenes

	ξ (eV)			$V_{sp\sigma}$	S^*
	Free atom	Normalised	Experimental	(eV)	$\Delta_R \neq 0$
Graphene	0.006	0.009	-	5.580	0.999 [0.999]
Silicene	0.028	0.044	(-) 0.044	2.54	0.999 [0.999]
Germanene	0.2	0.29	(0.2) 0.29	2.36	0.996 [0.993]
Stanene	0.6	0.8	(0.48) 0.77	1.953	0.961 [0.934]
Arsenene	0.26 (0.36)	0.421	-	1.275	0.978 [0.955]
Antimonene	0.6 (0.8)	0.973	-	1.170	0.904 [0.802]
Bismuthene	1.5	2.25	-	1.3	0.707 [0.568]

Assuming $dz \approx z$ and $\sin\theta \approx 1$ for quasi-planar/low-buckled honeycomb lattice).
Similar to other group-IV and V elements, a normalization factor of 3/2 is assumed for bismuthene compared to the free atomic SOI.

[0057] Modelling results for an NC-TQFET which is a strongly spin-orbit coupled version of BLG with similar screening properties but $S^* = 0.57$, equivalent to the spin-orbit parameters for bismuthene, yield an $E_g(V_g)$ given by the solid upper curve in **Figure 4**.

[0058] **Figure 4** also allows a comparison between the modelled NC-TQFET with a hypothetical low voltage Complementary metal–oxide–semiconductor device (CMOS LV) which corresponds to a gate-all-around field effect transistor (GAAFET) at the 2018 node (metal-1 half-pitch F = 15 nm). CMOS LV characteristics are $V_g = 0.3$ V, on current $I_{on} = 3.2$ μA, on-off ratio $I_{on}/I_{off} = 1.3 \times 10^4$, intrinsic device switching energy $E_{int} = 3.62$ aJ and intrinsic delay time $\tau = 3.8$ ps. For the purpose of the comparison, the inventors have assumed that the off current is $I_{off} = I_{on}\exp(-E_g/kT)$ where the I_{on} is the current at $E_g = 0$, $kT = 26$ meV is the thermal energy at room temperature, which corresponds to $E_g = 245$ meV. From **Figure 4** it can be seen that BLG has $E_g = 245$ meV at $V_g = 0.213$ V, only a modest improvement over CMOS LV. However, the modelled

bismuthene NC-TQFET has E_g = 245 meV at V_g = 0.030 V. This represents an order-of-magnitude improvement over CMOS LV.

[0059] For the purpose of the modelling, the inventors have further assumed that the NC-TQFET has a width F and gate length F = 15 nm. The on-state occurs at zero bandgap, where the BLG is a massive Dirac semimetal with a conductivity approximately 4 e^2/h and conductance 155 μS. Drain voltage $V_d = V_g$ = 0.030 V gives I_{on} = 4.6 μA, similar to CMOS LV. The gate charge Q is 6.0 x 10^{-17} C = 374 e, where e is the elemental charge, and the intrinsic switching energy E_{int} = $(1/4)QV_g$ = 0.45 aJ. The channel resistance R = 6.45 kOhms, and gate capacitance $C = Q/V_g$ = 2000 aF, giving the switching time $\tau = (RC)$ = 13 ps. The intrinsic switching energy of 0.45 aJ is almost an order of magnitude lower than CMOS LV.

[0060] As shown in **Figure 4**, if a ferroelectric with a higher remnant polarization is used, such as $BiFeO_3$ (P_r = 130 μC/cm^2) then a larger bandgap may be achieved at smaller gate voltages (dotted lines).

[0061] The NC-TQFET points to a general strategy to realize a new type of low-voltage transistor. The operating parameters of such a transistor are set by the materials parameters of the 2D TI and ferroelectric layers, and there appears to be no fundamental lower bound to the subthreshold swing for such a device.

[0062] It will be understood that the invention disclosed and defined in this specification extends to all alternative combinations of two or more of the individual features mentioned or evident from the text or drawings. All of these different combinations constitute various alternative aspects of the invention.

CLAIMS

1. A structure comprising: a top gate electrode and a bottom gate electrode, a channel layer formed from a channel material with a band gap modulable by electric field, the channel layer being electrically insulated from the top gate electrode and the bottom gate electrode and being located adjacent to at least one layer of a negative capacitance material.

2. A structure comprising:

a top gate electrode and a bottom gate electrode,

a planar channel layer located between the top gate electrode and the bottom gate electrode, the planar channel layer being separated from the top gate electrode by a first insulating layer and separated from the bottom gate electrode by a second insulating layer;

wherein the planar channel layer is formed from a channel material with a band gap modulable by electric field;

wherein at least one of the first insulating layer and the second insulating layer are formed from a negative capacitance material.

3. The structure of claim 2, wherein both of the first insulating layer and the second insulating layers are formed from the ferroelectric material.

4. The structure of claim 2 or 3 wherein the negative capacitance material exhibits negative capacitance and wherein the channel material exhibits positive capacitance, and the combined capacitance of the channel layer, the first insulating layer, and second insulating layer is greater than 0.

5. The structure of any one of claims 2 to 4, wherein the first insulating layer and the second insulating layer are each in physical contact with the planar channel layer, the first insulating layer being arranged on a first side of the planar channel layer and the second insulating layer being arranged on a second side of the planar channel layer.

6. The structure of any one of the preceding claims, wherein the top gate and the bottom gate are operable independently of one another.

7. The structure of any one of the preceding claims, wherein the structure further comprises a source electrode in electrical contact with the channel layer, and a drain electrode spaced apart from the source electrode and in electrical contact with the channel layer.

8. The structure of claim 7, wherein the source electrode is in electrical contact with the channel layer via a doped semiconductor material, and/or the drain electrode is in electrical contact with the channel layer via a doped semiconductor material.

9. The structure of claim 7, wherein the source electrode is formed from a doped semiconductor material and/or the drain electrode is formed from a doped semiconductor material.

10 The structure of any one of the preceding claims, wherein the top gate electrode and the bottom gate electrode are configured to apply an electric field across the channel layer in a direction perpendicular to a plane of the channel layer.

11. The structure of any one of the preceding claims, wherein the channel material is selected from the group consisting of: few-layer graphene, a two-dimensional semiconductor, or a topological material.

12. The structure of claim 11, wherein the channel material is a topological material.

13. The structure of claim 12, wherein the topological material is in the form of a thin film with a thickness of two unit cells or less.

14. The structure of claim 12 or 13, wherein the topological material exhibits a topological phase transition between a trivial state and a non-trivial state at a critical electric field strength.

15. The structure of any one of claims 12 to 14, wherein the topological material has a staggered honeycomb lattice structure.

16. The structure of any one of claims 12 to 14, wherein the topological material is a topological Dirac semimetal or a topological insulator.

17. The structure of any one of the preceding claims, wherein the planar channel layer is in the form of a thin film having a thickness of less than 10 nm.

18. The structure of any one of the preceding claims, wherein the structure is a field effect transistor or a component thereof.

19. A method of operating a structure according to any one of claims 1 to 18, the method comprising:

applying or modulating a gate voltage to the top gate electrode and/or the bottom gate electrode to generate or vary an electric field across the channel layer in a direction perpendicular to a plane of the channel layer to alter the bandgap of the channel material in the channel layer.

20. The method of claim 19, wherein altering the bandgap of the channel layer further comprises switching the channel material between a trivial state and a non-trivial or topological state.

21. Use of a structure according to any one of claims 1 to 18 in an electrical device.

22. An electrical device comprising the structure according to any one of claims 1 to 18.