

PATENT SPECIFICATION

(11) 1 266 017

DRAWINGS ATTACHED

1 266 017

- (21) Application No. 26107/69 (22) Filed 22 May 1969
(31) Convention Application No. 38895 (32) Filed 5 June 1968 in
(33) Japan (JA)
(45) Complete Specification published 8 March 1972
(51) International Classification H 03 k 23/02 3/02
(52) Index at acceptance

H3T 1P5 1PX 2B3 2F1 2F5 2J 2T2X 2T3F 3F1 3X 4C
4S 4X 5E
G4A 10EX 14 1C1B 1C5Y 8C



(54) IMPROVEMENTS IN OR RELATING TO TIMING PULSE GENERATORS

(71) We, OMRON TATEISI ELECTRONICS Co., a Japanese Body Corporate, of 10, Tsuchido-cho, Hanazono, Ukyoku, Kyoto, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a timing pulse generator for use in electronic calculators and more specifically to a timing pulse generator which is applicable to two-phase shift registers.

According to the present invention there is provided a timing pulse generator, wherein a plurality of two-phase shift registers and a pulse generating means are provided, said pulse generating means generates alternately read-in pulses for the first one of the shift registers and memory pulse for all the shift registers, each said shift register furnishes an output in response to respective read-in pulses and memory pulses, said output being provided in response to the absence of the output in each stage excluding the last stage and circulated to the input of the register as the data input of the shift register and the logical product of the output of the last stage of each shift register and the read-in pulse thereto is fed to the subsequent shift register as the read-in pulse thereto.

Further detailed description will be made in conjunction with a preferred embodiment of the invention with reference to the accompanying drawings, in which:—

Figure 1 shows a block diagram of an embodiment of the present invention.

Figure 2 illustrates a circuit diagram of any one stage of a two-phase dynamic type shift register for use in practising the present invention and

Figure 3 shows wave forms with reference to the output of each shift register

Referring to Fig. 1, two-phase dynamic type shift registers 1 and 2, each employing metal oxide semi-conductor field effect trans-

sistors, are respectively constituted of four stages, being first, second, third and fourth stages; the output of each stage except for the last stage is connected to the input of the first stage through NOR circuits 3 and 4 respectively.

In such shift registers 1 and 2 having four stages as illustrated, therefore, the input to the first stage will be zero when there is an output in any one of the first, second and third stages. Each stage of the shift register has an input section to which input data is transferred in response to a read in pulse from a pulse generator 7 and an output section to which data is transferred from the input section in response to a memory pulse from the pulse generator 7. ϕ_1 shows the read-in pulses for the shift register 1 and ϕ_2 shows the memory pulses commonly applicable to both shift registers 1 and 2.

The pulses ϕ_1 and ϕ_2 are generated alternately by means of the pulse generator 7. The pulses ϕ_1 are fed also to an AND circuit 5, which is further supplied with the output of the last stage of the shift register 1. The logical product of the output of the last stage of the shift register 1 and the read-in pulse ϕ_1 becomes the output ϕ_1^1 of the AND circuit 5 and the output ϕ_1^1 is fed to the subsequent shift register 2 as a read-in pulse. An AND circuit 6 is furnished with the output of the last stage of the shift register 2 and the read-in pulse ϕ_1^1 , the logical product of which is obtained as the output ϕ_1^{11} of the AND circuit 6; the output ϕ_1^{11} is fed to a subsequent shift register (not illustrated) which is similar to shift register 2 and operates in the same manner as shift register 2 as a read-in pulse.

Fig. 2 shows the connection of one stage of the two-phase dynamic type shift register 1. The connection of all stages of the shift register is the same. The memory pulses ϕ_2 are applied to all these stages, whereas the read-in pulses ϕ_1 are fed to each stage of the shift register 1 and the read-in pulses

ϕ_1 are fed to each stage of the shift register 2.

Referring to Fig. 2, 10, 11, 12, 13, 14 and 15 denote a metal oxide semi-conductor field effect transistor, which is shortly referred to as MOST throughout the present specification.

The drain of the MOST 10 is connected to the gate of the MOST 11, the source of which is kept at a positive potential and the drain of which is connected to the source of the MOST 12 and the source of the MOST 13. The drain of the MOST 13 is connected to the gate of the MOST 14, the source of which is kept at a positive potential and the drain of which is connected to the source of the MOST 15. Gates and drains of the MOST's 12 and 15 are kept at a negative potential. An input is fed to the source of the MOST 10, the read-in pulses ϕ_1 are fed to the gate of the MOST 10 and the memory pulses ϕ_2 are fed to the gate of the MOST 13. The MOST's 12 and 15 are utilized as load MOST.

Supposing that an input is supplied to the stage as shown in Fig. 2, the input is read in to a capacitance C_1 as illustrated by a broken line between the gate and the source of the MOST 11 on the strength of each of the read-in pulses ϕ_1 and is then transferred to a capacitance C_2 as illustrated by a broken line between the gate and the source of MOST 13 in response to each of the memory pulses ϕ_2 to provide an output of this stage.

Now with reference to Fig. 3, the operation of an apparatus as shown in Fig. 1 will be explained. Supposing that there is no output in any one of the first, second and third stages of the shift register 1, an output is obtained from the NOR circuit 3 and is fed as an input to the first stage of the shift register 1. The input is read in at the first stage on the strength of the read-in pulse ϕ_1 —1 as shown in Fig. 3 and is then taken out as an output of the following memory pulse ϕ_2 —1. The read-in pulse ϕ_1 —1 is fed during the middle portion of the duration of the output of the first stage. The presence of the output at the first stage makes the output of the NOR circuit 3 absent and accordingly makes the input to the first stage absent. The output of the first stage is read in to the second stage in response to the following read-in pulse ϕ_1 —2 and is then taken out as an output of the second stage in response to the following memory pulse ϕ_2 —2. The read-in pulse ϕ_1 —2 is fed during the middle portion of the duration of the output of the second stage. At that time there is no output at the first stage, but the output of the NOR circuit is also zero due to the output from the second stage, resulting in no input to the first stage.

Similarly, an output of the second stage is read in to the third stage and is further taken out as an output of the third stage, at which time the output of the second stage becomes zero, resulting in no output neither in the first stage nor in the second stage. But as the output of the NOR circuit 3 is made zero due to the output of the third stage, there is no input to the first stage.

Further, the read-in pulse ϕ_1 —4 is supplied in the middle portion of the duration of the output of the third stage, which is read in to the fourth stage to provide an output from the fourth stage, at which time no output is obtained from any one of the first through third stages, resulting in an output from the NOR circuit 3 to be fed to the first stage.

Thus the stage that furnishes the output is circulated and one cycle operation of the shift register 1 ends with a one time circulation. When the read-in pulse ϕ_1 —5 is fed, the input is read in to the first stage of the shift register 1 and the subsequent cycle of the shift register 1 begins.

As soon as the subsequent cycle begins, the logical product of the output from the fourth or last stage and the read-in pulse ϕ_1 —5 is obtained by means of the AND circuit 5 to furnish an output pulse ϕ_1 —1. The output pulse ϕ_1 —1 is utilized as a read-in pulse to be fed to the first stage of the subsequent shift register 2 and becomes an output of the stage on the strength of the next memory pulse ϕ_2 —5. When an output is obtained at the fourth stage during the subsequent cycle of the shift register 1, the logical product of the output and the subsequent read-in pulse ϕ_1 —9 to be fed to the shift register 1 is obtained in the AND circuit 5 to furnish an output pulse ϕ_1 —2, in response to which the output of the first stage of the shift register 2 is read in to the second stage thereof and the output of the first stage of the shift register 2 becomes zero in response to the subsequent memory pulse ϕ_2 —9, resulting in an output at the second stage thereof. Thus, the shift register 2 makes one-cycle of operation during every four cycles in the shift register 1 in response to the read-in pulses ϕ_1 and the memory pulses ϕ_2 .

Since the operation of the shift register 2 is equivalent to that of the shift register 1, detailed explanation thereof is omitted.

A logical product of the output from the last stage of the shift register 2 and one of the read-in pulses ϕ_1 is obtained from the AND circuit 6 to furnish the output pulse ϕ_1 —11, which is utilized as a read-in pulse to the subsequent shift register (not shown). The subsequent shift register is the same as shift register 2, and the operation thereof is the same as shift register 2. It will be appreciated that any number of such shift regi-

sters connected as shown in the drawings may be utilised.

Thus, a plurality of two-phase dynamic type shift registers are connected as described above and furnish an output in response to the read-in pulses and the memory pulses fed to the said shift register, the output being circulated through the stages. The logical product of the output from the last stage in each shift register and the read-in pulse is utilized as a read-in pulse for the subsequent shift register and an output from a certain shift register is carried over to the subsequent shift register, which makes it possible to provide the timing pulses of desired pulse width.

As clearly shown in Fig. 3, each of the read-in pulses ϕ_1 is supplied in the middle portion of the duration of the respective output of the each stage of the shift register 1 and especially ϕ_1-5 , ϕ_1-9 etc. are supplied in the middle portion of the duration of the respective output of the fourth stage. This fact makes it possible that the output ϕ_1^1 from the AND circuit 5 is always stabilized even in case the wave form of output from the shift register 1 is distorted.

Similarly, the output ϕ_1^{11} from the AND circuit 6 is stabilized and the stabilized read-in pulses for the subsequent shift register can always be obtained.

WHAT WE CLAIM IS:—

1. A timing pulse generator, wherein a plurality of two-phase shift registers and a pulse generating means are provided, said pulse generating means generates alternately read-in pulses for the first one of the shift registers and memory pulses for all the shift registers, each said shift register fur-

nishes an output in response to respective read-in pulses and memory pulses, said output being provided in response to the absence of the output in each stage excluding the last stage and circulated to the input of the register as the data input of the shift register and the logical product of the output of the last stage of each shift register and the read-in pulse thereto is fed to the subsequent shift register as the read-in pulse thereto.

2. A timing pulse generator comprising a plurality of two-phase shift registers, pulse generating means for generating alternately read-in pulses for the first shift register and memory pulses for all shift registers, NOR circuits arranged correspondingly to each of said shift registers and supplied with the output from all stages excluding the last stage of a respective shift register so as to furnish the output thereof to the first stage of the corresponding shift register, and AND circuits arranged correspondingly to each of said shift registers for furnishing the logical product of the output of the last stage of each shift register and the read-in pulse to the subsequent shift register as a read-in pulse thereto.

3. A timing pulse generator substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

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Similarly, the output ϕ_1 from the AND circuit 6 is stabilized and the stabilized read-in pulses for the subsequent shift register can always be obtained.

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1. A timing pulse generator, wherein a plurality of two-phase shift registers and a pulse generating means are provided, said pulse generating means generates alternately read-in pulses for the first one of the shift registers and memory pulses for all the shift registers, each said shift register fur-

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2. A timing pulse generator comprising a plurality of two-phase shift registers, pulse generating means for generating alternately read-in pulses for the first shift register and memory pulses for all shift registers, NOR circuits arranged correspondingly to each of said shift registers and supplied with the output from all stages excluding the last stage of a respective shift register so as to furnish the output thereof to the first stage of the corresponding shift register, and AND circuits arranged correspondingly to each of said shift registers for furnishing the logical product of the output of the last stage of each shift register and the read-in pulse to the subsequent shift register as a read-in pulse thereto.

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