

PATENT APPLICATION
DOCKET NO.: 100202127-1

ABSTRACT

PHASE DETECTOR FOR A PROGRAMMABLE CLOCK SYNCHRONIZER

A phase detector (130) in a programmable clock synchronizer (100) for effectuating data transfer between first circuitry (103A) disposed in a first clock domain and second circuitry (103B) disposed in a second clock domain. The phase detector (130) includes a series of flip flops (204, 206, 212, 214, 220) disposed in parallel that sample the second clock signal (108) with both a rising edge of the first clock signal (106) and a falling edge of the first clock signal (106). By tracking movement in one-to-zero or zero-to-one transitions in the sampled clock signals (210, 222), the phase detector (130) is operable to determine the phase difference between the first and second clock signals (106, 108).

(FIG. 2)