CLAIMS

1. A wake-up circuit comprising:

a first comparator coupled to an input signal and configured to compare the input signal to a first comparison value;

a second comparator coupled to the input signal and configured to compare the input signal to a second comparison value;

an exclusive OR gate, a first input of the exclusive OR gate coupled to an output of the first comparator, a second input of the exclusive OR gate coupled to an output of the second comparator; and

a tunable charge pump coupled to an output of the exclusive OR gate, the tunable charge pump comprising a p-type metal oxide semiconductor (PMOS) transistor controlled by the output of the exclusive OR gate and at least one n-type metal oxide semiconductor (NMOS) transistor controlled by the output of the exclusive OR gate and configured to convert a signal from the exclusive OR gate to a direct current (DC) value to wake up a circuit being monitored.

2. The wake-up circuit of claim 1, further comprising a buffer configured to convert the DC value to a digital voltage level.

3. The wake-up circuit of claim 2, wherein the buffer comprises an inverter.

4. The wake-up circuit of claim 1, further comprising an input switch configured to isolate the input signal for DC calibration.

5. The wake-up circuit of claim 4, further comprising a DC block capacitor coupling the input switch to the input signal.

6. The wake-up circuit of claim 5, further comprising a DC set circuit.

7. A method to wake up a circuit, the method comprising:

comparing an input signal to a first comparison value to generate a first comparison result;

comparing the input signal to a second comparison value to generate a second comparison result;

combining the first comparison result and the second comparison result to generate a signal;

converting the signal to a direct current (DC) value by controlling a tunable charge pump comprising a p-type metal oxide semiconductor (PMOS) transistor and at least one n-type metal oxide semiconductor (NMOS) transistor using the combined first comparison result and the second comparison; and

waking up the circuit based on the DC value.

8. The method of claim 7, further comprising buffering the DC value to convert the DC value to a digital voltage level.

9. The method of claim 8, further comprising buffering the DC value using an inverter.

10. The method of claim 7, further comprising switching the input signal to isolate the input signal for DC calibration.

11. The method of claim 10, further comprising DC filtering the input signal to generate a DC filtered input signal.

12. The method of claim 11, further comprising DC setting the DC filtered input signal.

13. A wake-up circuit comprising:

means for comparing an input signal to a first comparison value to generate a first comparison result;

means for comparing the input signal to a second comparison value to generate a second comparison result;

means for combining the first comparison result and the second comparison result to generate a signal;

means for converting the signal to a direct current (DC) value by controlling a tunable charge pump comprising a p-type metal oxide semiconductor (PMOS) transistor and at least one n-type metal oxide semiconductor (NMOS) transistor using the combined first comparison result and the second comparison; and

means for waking up a circuit based on the DC value.

14. The wake-up circuit of claim 13, further comprising means for buffering the DC value to convert the DC value to a digital voltage level.

15. The wake-up circuit of claim 14, wherein the means for buffering the DC value comprises an inverter.

16. The wake-up circuit of claim 13, further comprising means for switching the input signal to isolate the input signal for DC calibration.

17. The wake-up circuit of claim 16, further comprising means for DC filtering the input signal to generate a DC filtered input signal.

18. The wake-up circuit of claim 17, further comprising means for DC setting the DC filtered input signal.