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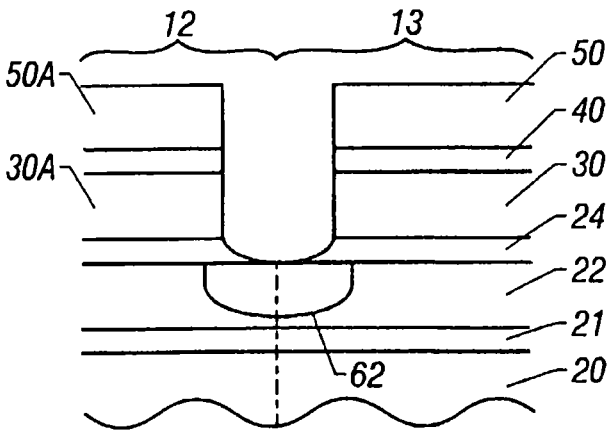
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(54) Title: SINGLE TUNNEL GATE OXIDATION PROCESS FOR FABRICATING NAND FLASH MEMORY



(57) Abstract: A single tunnel gate oxidation process for fabricating NAND memory strings where the gate oxide (24) of the select transistors and the floating gate memory transistors are fabricated in a single oxidation step is disclosed. The select gate transistors and the floating gate memory transistors have an oxide thickness of 85Å-105Å. For single tunnel gate approach, a careful selection of the medium doped source/drain region (62) implant conditions is necessary for proper function of the NAND memory string. In one embodiment, the medium doped source/drain region is doped with Arsenic to a concentration of 10^{13}-10^{14}/cm^2.

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