

IMPROVEMENTS IN OR RELATING TO
TRANSVERSAL EQUALISERS

The present invention relates to transversal equalisers and more particularly d.c. compensation in adaptive equalisers.

The presence of a d.c. offset in an input signal to an adaptive equaliser causes confusion in the coefficient update algorithm because the error signal does not correlate properly with the data signal samples at each tap of the equaliser. The d.c. offset in the input signal has therefore to be reduced to zero before the signal enters the equaliser. This is normally accomplished by using adjust-on-test resistors or potentiometers providing in-life adjustments to correct for ageing drift in analogue components such as operational amplifiers, sample-and-hold circuits and the analogue-to-digital converter itself.

According to the present invention there is provided an adaptive equaliser including a plurality of tap stages, the first stage receives an input signal and subsequent stages receive time spaced samples of the input signal and each stage includes a multiplier and a correlator both of which are fed by an input signal, the output signal from the multiplier are summed by an accumulator which applies a signal to a decision circuit providing an output signal and an error signal, the latter is applied to each correlator to correct residual error, said adaptive equaliser includes an additional tap stage having its respective multiplier and correlator connected to a fixed voltage source, the

output signal from the multiplier is summed with the other multiplier output signals by said accumulator and the error signal produced by said decision circuit is correlated with said fixed voltage by the additional correlator to control the gain of the additional tap stage multiplier thereby compensating for an original d.c. offset in the input signal.

According to a feature of the invention the adaptive equaliser finds application in modulator/demodulator equipment commonly known as modems.

The invention will be readily understood from the following exemplary embodiment thereof and should be read in conjunction with the following drawing wherein:-

Figure 1 shows a known form of adaptive equaliser; and,

Figure 2 shows an adaptive equaliser in accordance with the present invention.

Referring to Figure 1 the time-spaced samples of the input signal x_i , $x(i-T)$, $x(i-2T)$ are multiplied by the four-quadrant multipliers M_1 , M_2 , and M_3 respectively and then summed in an accumulator A. The output of accumulator A is fed to decision circuit D and compared with a set of reference levels or with a locally generated reference signal to produce an output signal Y_K and error signal E_K . The error signal E_K is correlated with the signal samples in the correlators C1, C2 and C3 respectively, the outputs of which control the gains of associated multipliers M_1 , M_2 and M_3 to minimise the correlation of each tap.

If there is a d.c. offset in the input signal the correlators C_1 , C_2 and C_3 will attempt to correct the residual error, but since there is no linear relationship between the d.c. offset and the signal samples the effect of this attempt to remove the d.c. offset will result in non-optimum settings for the multipliers M_1 , M_2 and M_3 and distortion in the output signal Y_K will occur.

Referring to Figure 2 an equaliser according to the invention is shown which includes a fourth tap connected to a fixed voltage source V . The voltage V is multiplied by a multiplier M_4 and summed with the outputs of multipliers M_1 , M_2 and M_3 by accumulator A . The error signal E_K is correlated with the fixed voltage V in the correlator C_4 . The output of correlator C_4 is used to control the gain of multiplier M_4 until the d.c. offset of the output of accumulator A is reduced to zero, allowing multipliers M_1 , M_2 M_3 to assume their optimum gain values.

The above description has been of one embodiment only and is not intended to limit the scope of the invention.

For example, the invention could be applied to adaptive equalisers having complex-valued tap gain coefficients by having two additional taps as described, one to remove the d.c. in the inphase channel and one to remove the d.c. in the so-called Quadrature channel.



CLAIMS

1. An adaptive equaliser including a plurality of tap stages, the first stage receives an input signal and subsequent stages receive time spaced samples of the input signal and each stage includes a multiplier and a correlator both of which are fed by an input signal, the output signals from the multipliers are summed by an accumulator which applies a signal to a decision circuit providing an output signal and an error signal, the latter is applied to each correlator to correct residual error, said adaptive equaliser includes an additional tap stage having its respective multiplier and correlator connected to a fixed voltage source, the output signal from the multiplier is summed with the other multiplier output signals by said accumulator and the error signal produced by said decision circuit is correlated with said fixed voltage by the additional correlator to control the gain of the additional tap stage multiplier thereby compensating for an original d.c. offset in the input signal.
2. An adaptive equaliser as claimed in claim 1, in which the additional correlator controls the gain of the additional tap stage multiplier until the d.c. offset is reduced to zero, allowing the multipliers of the other tap stages to assume their optimum gain values.
3. A modulator/demodulator including an adaptive equaliser as claimed in claim 1 or 2.
4. An adaptive equaliser substantially as described with reference to the accompanying drawing.