

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a memory cell array, an ECC engine, a voltage generator and a control logic circuit. The memory cell array includes a plurality of memory cells coupled to word-lines and bit-lines, and a plurality of sense amplifiers to sense data stored in the plurality of memory cells. The ECC engine reads memory data from a target page of the memory cell array, performs an ECC decoding on the memory data, detects, based on the ECC decoding, an error in the memory data, and outputs error information associated with the error. The voltage generator provides driving voltages to the plurality of sense amplifiers, respectively. The control logic circuit controls the ECC engine, and controls the at least one voltage generator to increase an operating margin of each of the plurality of sense amplifiers based on error pattern information including the error information.

Fig. 2