

Overcurrent and midpoint voltage detection

The present invention relates to inverters having half-bridge circuits, to an electronic ballast (EVG) for gas
5 discharge lamps having such an inverter, to methods for monitoring the condition of an inverter having a half-bridge circuit, and to a computer software program product which supports such methods when it is run by means of a computer.

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The background to the present invention is for example the field of application of electronic ballasts. Such electronic ballasts are well known from the state of the art and conventionally have a rectifier, supplied with
15 mains voltage, having PFC (power factor correction). The d.c. voltage generated by this unit is then delivered to a half-bridge clocked with high frequency, which generates a high frequency a.c. voltage, which in turn is delivered to at least one connected gas discharge lamp.
20 The half-bridge circuit thereby has as a rule two switches connected in series, such as for example power transistors, which are clocked by means of a control unit, such as for example ASIC.

25 In the switching processes of these power transistors of the half-bridge attention is to be paid to the fact that a so-called "hard switching" is avoided. "Hard switching" thereby means that during the free-wheeling phase of the current through the half-bridge, through the free-
30 wheeling diode (parallel to the switch and possibly integrated therein), the opposing switch is switched on. Thereby, damage to the switch can arise.

From the state of the art there are known suggestions to deactivate the half-bridge after the occurrence of such a hard switching procedure.

5 On the other hand it is also known for example from WO 00/35252 (see Figure 14 there), to monitor the condition of the half-bridge circuit, and more precisely stated the voltage at the midpoint between the two switches, wherein thereby the appropriate transistor is only then switched
10 on when the free-wheeling phase has ended. A disadvantage of this circuit is that for monitoring this midpoint voltage at a control unit, for example at the same control unit which also controls the switches, an additional pin of an integrated circuit is occupied.

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Starting from this state of the art it is thus the object of the present invention to propose a more effectively configured monitoring and control circuit for a half-bridge.

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This object is achieved in accordance with the invention by means of the features of the independent claims. The dependent claims further develop the central concept of the present invention in a particularly advantageous
25 manner.

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In accordance with the invention it is thereby made possible that the pin of an integrated circuit needed for monitoring the midpoint voltage of the half-bridge can simultaneously also be employed for monitoring the current of the half-bridge. In accordance with the invention, thereby the monitoring circuit is so configured that on the one hand in one phase of the

clocking of the switches the measurement signal at a pin of the integrated circuit is employed as a midpoint voltage. In a phase of the clocking of the switches (power transistors) temporally separated therefrom, the same pin can on the other hand be employed for determination of the half-bridge current. The current through the half-bridge may thereby for example be employed for detection of an over-current condition and for lamp power regulation.

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In accordance with a first aspect of the present invention there is thus proposed an inverter having a half-bridge circuit, which has two switches connected in series and supplied with d.c. voltage, at the midpoint of which, with appropriate counter-clocking of the circuit, and a.c. voltage is made available. Further, a control unit is provided which clocks the switches and evaluates a measurement signal tapped off at the midpoint in different temporal phases of the clocking of the switches for detection of the current through the half-bridge and for detection of the voltage at the midpoint.

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The control unit may thereby evaluate the midpoint signal as current through the half-bridge when only the switch of the half-bridge lying at low potential is closed.

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On the other hand, the control unit can evaluate the midpoint signal as voltage value of the midpoint in a temporal phase of the clocking in which at least the switch lying at lower potential is open. In particular the control unit can evaluate the midpoint signal thereby as voltage value of the midpoint during a dead time, in which both switches are open.

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The dead time may thereby be variable by means of the control unit in dependence upon the detected midpoint voltage, in particular extendable, starting from a standard setting.

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The potentially lower switch may be connected with ground by means of an Ohmic measurement resistance, whereby the resistance value of the measurement resistance is substantially smaller than the resistance of the
10 potentially lower switch in the closed condition of the switch.

A further Ohmic resistance can be connected parallel to the potentially lower switch, whereby the midpoint signal
15 between the measurement resistance and the potentially lower switch is tapped off.

A comparator for comparison of the measurement signal with a reference voltage may be provided, whereby then
20 the result of the comparison is passed on to the control unit for further evaluation.

The control unit may for example be an ASIC.

25 The control unit may switch on a switch first when the detection of the midpoint voltage has indicated that the free-wheeling phase of the half-bridge current has ended, and thus a potential-less switching procedure is ensured.

30 In accordance with a further aspect of the present invention there is provided an electronic ballast for gas discharge lamps having such an inverter.

Finally, the invention relates to methods for monitoring the condition of an inverter having a half-bridge circuit.

5 Further features, advantages and characteristics of the present invention will now be described in more detail with reference to the accompanying Figures and by detailed description of different exemplary embodiments of the present invention.

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Figure 1a thereby shows a first exemplary embodiment of the invention in the condition in which, during a so-called dead time, a midpoint voltage measurement is effected,

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Figure 1b shows the condition of the first exemplary embodiment during a measurement of the current through the half-bridge,

20 Figure 2a shows a second exemplary embodiment of the present invention in the condition in which, during the dead time, the voltage at the midpoint is measured, and

Figure 2b again shows the second exemplary embodiment in
25 a condition in which the current through the half-bridge is measured.

Figure 1a shows a first exemplary embodiment of the invention with an inverter 10 having a half-bridge
30 circuit 5, to which a DC bus voltage 3 is delivered. The half-bridge circuit 5 has two power switches 1, 2 in each case with free-wheeling diodes 11 and 12 connected parallel thereto. These free-wheeling diodes 11, 12 may

also be integrated in to the switches (transistors). By means of appropriate (high-frequency) clocking of the switches 1, 2 by means of the control unit 6, there is made available at the midpoint 4 of the half-bridge circuit 5 a (high-frequency) a.c. voltage, which for example is delivered to a choke 13 of a following load circuit, whereby this load circuit usually contains the lamp.

- 10 The task of a monitoring circuit connected to this half-bridge circuit 5 is on the one hand to avoid a so-called hard switching, i.e. a non-potential-less switching of the transistors 1, 2. The switches are switched in a potential-less manner when the free-wheeling diodes 11, 12 become capable of conduction in the inductive operating range of the half-bridge circuit, before the switches are switched on.

This is the case when resonance curves of the load circuit manifest an inductive behaviour. In contrast, this condition is no longer fulfilled if the load circuit shows a capacitive behaviour.

In accordance with the invention, thereby the midpoint voltage is measured in a temporal phase of the clocking of the switches 1, 2 in which at least the potentially lower switch 2 is open. In particular, however, this midpoint voltage measurement can be carried out during the dead time, during which thus both switches 1, 2 are open.

The monitoring circuit thereby has a first Ohmic resistance 8, which is connected parallel to the

potentially lower switch 2. This first Ohmic resistance 8 forms with an Ohmic measurement resistance 7, which connects the potentially lower switch 2 with ground, a voltage divider. The voltage divider signal is then
5 delivered to a comparator 9, which compares the voltage divider signal with a predetermined reference voltage V_{ref} and delivers the comparison signal to the control unit 6.

Since the control unit 6 determines the temporal clocking
10 of the switches 1, 2, an incoming measurement signal at pin 14 can be unambiguously associated with the dead time phase.

It is to be noted that the resistance value of the Ohmic
15 resistance 7 is significantly smaller than the switch resistance of the potentially lower switch 2 in closed condition (switched-on condition) and for example may be a few mOhm.

20 Thus, during the midpoint voltage measurement, preferably during the temporal duration of the dead time, the measurement of the half-bridge current is effected, as can be seen from Figure 1b, when the potentially lower switch 2, as predetermined by the control circuit 6, is
25 closed. In this condition, in which the midpoint voltage is about 0.7 volt, the half-bridge current is measured by means of the voltage at the measurement resistance 7 and in turn delivered to the comparator 9.

30 It is to be noted that the same circuit in Figure 1a and Figure 1b, with the employment of one and the same pin 14 of the circuit 6 can carry out on the one hand the midpoint voltage measurement in a first temporal phase of

the clocking of the switches 1, 2 and on the other hand the measurement of the current through the semiconductor bridge.

5 Figures 2a and 2b show a second exemplary embodiment of the invention, in which the monitored circuit is simplified insofar as the measurement signal is directly tapped off at the midpoint 4. Again, as can be seen in Figure 2a, the measurement of the midpoint voltage is
10 effected during the dead time, thus while both switches 1, 2 are open, and the measurement of the current through the half-bridge is effected during the temporal duration of the clocking of the switches 1, 2 whilst the potentially lower switch 2 is closed.

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The simplification of the circuit in accordance with Figures 2a and 2b, in comparison would the circuit in accordance with Figures 1a, 1b, thereby represents a compromise to the effect that the switch resistance of
20 the switch S2 (R_{S2on}) is only very crudely known, so that the current measurement in the condition of Figure 2b is relatively imprecise. Meanwhile, the precision with appropriate setting of a threshold value in the control circuit 6 is adequate in order to be able to effect a
25 security switching off in the event of an over-current recognition in the half bridge.

Alternatively, the switch S2 is also be formed as integrated switch, whereby in this case the switch
30 resistance in the closed condition (R_{S2on}) is relatively precisely defined, and thus also the current measurement in the example of Figure 2b can be effected more precisely.

The detection of the half-bridge current can, meanwhile, serve not only for a security switching off in the event of the detection of an over-current condition, but also
5 as at least one parameter of a lamp power regulation.

In accordance with the invention, thus, the pin number of the control IC 6 can be kept low since a measurement concept is proposed that in terms of circuitry technology
10 combines the detection of the midpoint voltage with the over-current detection in the half-bridge.

Since the midpoint voltage is always determined, before the corresponding transistor is switched on and on the
15 other hand a dead time is always present, measurement is effected in the current-less condition, which makes possible an additive superimposition of half-bridge current and midpoint voltage detection.

Claims

1. Inverter with a half-bridge circuit, having:

- 5 - two switches (1, 2) connected in series and supplied with d.c. voltage (3), at the midpoint (4) of which, with counter-clocking of the switches (1, 2), an a.c. voltage is made available and
- 10 - a control unit (6), which clocks the switches (1, 2) and evaluates a measurement signal tapped off at the midpoint (4) in different temporal phases of the clocking of the switches (1, 2) for detection of the current through the half-bridge (5) and of the voltage at the
- 15 midpoint (4).

2. Inverter according claim 1,

- characterised in that,
- 20 the control unit (6) evaluates the midpoint signal as current through the half-bridge (5), when only the switch (1) lying at lower potential is closed.

3. Inverter according to any preceding claim,

- characterize in that,
- 25 the control unit (6) evaluates the midpoint signal as voltage value of the midpoint (4) in a phase in which at least the switch (2) lying at lower potential is open.

- 30 4. Inverter according to claim 3, characterized in that,

the control unit (6) evaluates the midpoint signal as voltage value of the midpoint in a dead time, in which both switches (1, 2) are open.

- 5 5. Inverter according to claim 4,
characterized in that,
the dead time is variable in dependence upon the
detected midpoint voltage.
- 10 6. Inverter according to any preceding claim,
characterized in that,
the potentially lower switch (2) is connected with
ground by means of an Ohmic measurement resistance
(7), the resistance value of which is substantially
15 smaller than the resistance of the potentially lower
switch (2) in the closed condition.
- 20 7. Inverter according to claim 6,
characterized in that,
a further Ohmic resistance (8) is connected parallel
to the potentially lower switch (2) and the midpoint
signal is tapped off between the measurement
resistance and the potentially lower switch (2).
- 25 8. Inverter according to claim 7,
characterized by,
a comparator (9) for comparison of the measurement
signal with a reference voltage.
- 30 9. Inverter according to any preceding claim,
characterized in that,
the control unit is an ASIC.

10. Inverter according to any preceding claim,
characterized in that,
the control unit switches on a switch only then when
the detection of the midpoint voltage has indicated
5 that the free-wheeling phase of the half-bridge
current has ended, and thus a potential-less
switching procedure is ensured.
11. Electronic ballast for gas discharged lamp,
10 having an inverter (10) in accordance with any
preceding claim.
12. Method of monitoring the condition of an
inverter having a half-bridge circuit, which has two
15 switches (1, 2) connected in series and supplied
with d.c. voltage (3), at the midpoint (4) of which,
with appropriate counter-clocking of the switches
(1, 2), an a.c. voltage is made available,
characterized in that,
20 a measurement signal tapped off at the midpoint (4)
is evaluated in different temporal phases of the
clocking of the switches (1, 2) for the detection of
the current through the half-bridge (5) and of the
voltage at the midpoint (4).
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13. Method according to claim 12,
characterised in that,
the midpoint signal is evaluated as current through
the half-bridge (5) when only the switch (1) lying
30 at lower potential is closed.
14. Method according to any of claims 12 or 13,
characterized in that,

the midpoint signal is evaluated as voltage value of the midpoint (4) in a phase in which at least the switch (2) lying at lower potential is open.

- 5 15. Method according to any of claims 12 to 14,
characterized in that,
the midpoint signal is evaluated as voltage value of
the midpoint in a dead time, in which both switches
(1, 2) are open.
- 10 16. Method according to claims 15,
characterized in that,
the dead time is varied in dependence upon the
detected midpoint voltage.
- 15 17. Method according to any of claims 12 to 16,
wherein the potentially lower switch (2) is
connected with ground by means of an Ohmic
measurement resistance (7), the resistance value of
20 which is substantially smaller than the switch
resistance in closed condition, and a further Ohmic
resistance (8) is connected parallel to the
potentially lower switch (2),
characterized in that,
25 the midpoint signal is tapped off at a point between
the measurement resistance (7) and the potentially
lower switch (2).
- 30 18. Method according to claim 17,
characterized in that,
the measurement signal is compared with a reference
voltage.

19. Method according to any of claims 12 to 18,
characterized in that,
the voltage at the midpoint is evaluated for
ensuring potential-less switching procedures of the
switches (1, 2).
20. Method according to claim 19,
characterized in that,
a switch (1, 2) is only closed if the detection of
the midpoint voltage has indicated that the free-
wheeling phase of the half-bridge current has ended.
21. Method for controlling an inverter having a
half-bridge circuit, which has two switches (1, 2)
connected in series and supplied with d.c. voltage
(3), at the midpoint (4) of which, with appropriate
counter-clocking of the switches (1,2), an a.c.
voltage is made available,
characterized in that,
a measurement signal tapped off at the midpoint (4)
in a dead time, in which both switches (1, 2) are
open, is evaluated as voltage value of the midpoint
and this dead time is varied in dependence upon the
detected midpoint voltage.
22. Computer software program-product,
characterized in that,
it supports a method according to any of claims 12
to 20 when it is run by means of a micro-computer.
23. Inverter with a half-bridge circuit, having:
- two switches (1, 2) connected in series and
supplied with d.c. voltage (3), at the midpoint

(4) of which, with counter-clocking of the switches (1, 2), an a.c. voltage is made available and

- 5 - a control unit (6), which clocks the switches (1, 2) and evaluates a measurement signal tapped off at the midpoint (4) in a dead time, in which both switches (1, 2) are opened, as voltage value of the midpoint and sets the dead time in dependence upon the detected
- 10 midpoint voltage.