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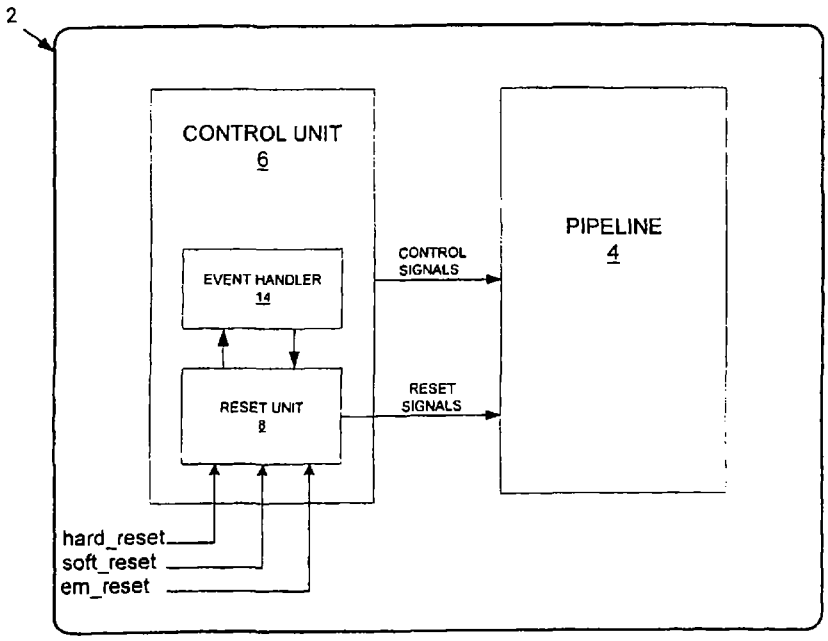
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(54) Title: RESETTING A PROGRAMMABLE PROCESSOR



(57) Abstract: In one embodiment, a pipelined processor includes a reset unit that provides an output reset signal to at least one stage of the pipeline. The reset unit is adapted to detect at least a hard reset request, a soft reset request and an emulation reset request. The pipeline comprises N stages and the reset unit asserts the reset signal for at least N cycles of a clock after the reset request has been cleared. Each stage if the pipeline has a storage circuit for storing a corresponding valid bit. At least one of the storage circuits is cleared in response to the reset signal. In addition, the reset unit handles the reset request as a reset event having an assigned priority.

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