

Semiconductor Device Fabrication

Abstract

5 There is provided a method for fabricating a
semiconductor device having the following structure, and
comprising the steps of growing a first and a second
nucleation layer on a substrate; depositing a binary layer
over these nucleation layers; and annealing the binary
10 layer to form a first contact area and a second contact
area on the substrate, wherein the annealed binary layer
comprises a group 14 element selected from Si, Ge and
their combination thereof, and the annealed binary layer
in the first and second contact areas are capable of
15 providing a lower contact resistance for a current to flow
in the device. This method serves to provide an
intermediate layer which enables the fabrication process
to become CMOS compatible.

20 (No suitable Figure)