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PATENT SPECIFICATION

958,245

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(Divided out of No. 958242).

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International Classification:—H 01 l.

COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Devices

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to semiconductor devices and more particularly to semiconductor devices having a configuration of regions for performing plural element circuit functions. The semiconductor device according to the invention may be an individual element such as a multi-emitter transistor for performing transistor and diode functions or a multi-emitter transistor formed as part of a semiconductor body containing other circuit elements as described in parent Patent Application No. 16071/60 (Serial No. 958,242) from which the present application is divided.

The present invention is a semiconductor device comprising an integral or integrated body of single crystal semiconductor material containing therein or thereon a first region of one conductivity type forming a part of one surface of said body, a second region of opposite conductivity type contiguous with said first region to form therewith a first P-N junction extending to said surface and there defining a first enclosed area within the periphery of said surface, a plurality of third regions of said opposite conductivity type contiguous with said first region to form therewith a respective plurality of P-N junctions each extending to said surface and there defining an enclosed area surrounded by said first enclosed area, and ohmic contacts to said first, second and third regions.

The present invention is also a semiconductor device comprising an integral or integrated body of single crystal semiconductor material containing therein or thereon discrete regions adapted to provide the electrical properties of a multi-emitter transistor and one or more other circuit elements, said multi-emitter transistor including a first region of one conductivity type forming a part of one surface of said body, a second region of opposite conductivity type contiguous with said first region to form therewith a first P-N junction extending to said surface and there defining a first enclosed area, a plurality of third regions of said opposite conductivity type contiguous with said first region to form therewith a respective plurality of P-N junctions each extending to said surface and there defining an enclosed area surrounded by said first enclosed area, and ohmic contacts to said first, second and third regions.

An embodiment of the invention will now be described by way of example with reference to the accompanying drawing, in which:—

Fig. 1 illustrates a top plan view of a semiconductor device embodying the invention;

Fig. 2A illustrates a schematic circuit diagram of the semiconductor device illustrated in Fig. 1;

Fig. 2B and 2C illustrate circuit diagrams showing variations in the circuit illustrated in Figs. 1 and 2A;

Fig. 3 shows a cross sectional view of one circuit element illustrated in Fig. 1 and an embodiment of the invention; and

Figs. 4 to 6, inclusive, show cross sectional views of some of the circuit elements illustrated in Fig. 1.

With reference to the drawings, embodiments of the invention will now be described in detail in order to provide a better under-

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standing of the principles of the invention and various forms and embodiments thereof.

With reference to Fig. 3, there is illustrated a multi-emitter transistor which may be part of a semiconductor body containing other circuit elements as illustrated in Figs. 1 to 2C and described in detail in said parent patent application.

The body of semiconductor material is of single crystal structure and can be composed of any suitable semiconductor material such as germanium, silicon, intermetallic alloys such as gallium arsenide, aluminum antimonide, indium antimonide, as well as others.

The multi-emitter transistor TR2 includes an N-type region 18 provided in the wafer 12, a P-type base region 20 and two N-type emitter regions 22 and 24. Ohmic contacts 26, 28 and 30 may be plated or evaporated onto their corresponding semiconductor regions. Collector lead 33 may be soldered or alloyed to substrate 10, and extends beneath the left-hand end of wafer 12 and makes ohmic contact therewith. The semiconductor device illustrated in Fig. 3 is a double emitter transistor and provides one NPN transistor plus an integral diode formed by the additional emitter region. The base and emitter regions may be formed by selective diffusion into the wafer 12.

The transistor TR3 illustrated in Fig. 1 is identical with TR2 illustrated in Fig. 3.

The multi-emitter transistor, Fig. 3, may have its collector region 18 mounted or secured to a substrate 10 which substrate may be intrinsic semiconductor material having a relatively high order of resistivity or the entire unit could be formed from a block of intrinsic semiconductor material into which doping impurities are diffused in the region occupied by the collector. According to the latter arrangement, the substrate 10 would be part of the same physical piece of semiconductor material as collector 18 and differing therefrom only in its electrical characteristics due to the impurity doping.

The multi-emitter transistor illustrated in Fig. 3 may be integrated with other circuit elements in a body of semiconductor material as described in said parent patent application wherein the manufacture and construction of semiconductor devices illustrated in Figs. 1 to 2C and 4 to 6 are described in detail. The collector-base P-N junction extends to one surface of the body and there defines an enclosed area and each emitter-base P-N junction extends to said one surface and there defines another enclosed area surrounded by said first-mentioned enclosed area. Therefore, the multi-emitter transistor illustrated in Fig. 3 may be combined with other circuit elements such as multi-emitter transistor TR3, diffused resistors R1 and R3, capacitors C1 and C2, diodes D2 and D3, and transistor TR1.

It must be emphasized that only several embodiments of the invention have been described and that other variations and modifications thereof may be made without departing from the scope of the invention which is defined in the appended claims.

Reference is additionally made to our copending patent applications nos. 23279/63; 46087/63; 46088/63; 46089/63; and 46090/63, (Serial nos. 958244, 958246, 958247, 958248 and 958249), also divided from said parent application no. 16071/60 with(Serial no. 958242).

Terms indicative of position, such as "thereon", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilised in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising an integral or integrated body of single crystal semiconductor material containing therein or thereon a first region of one conductivity type forming a part of one surface of said body, a second region of opposite conductivity type contiguous with said first region to form therewith a first P-N junction extending to said surface and there defining a first enclosed area within the periphery of said surface, a plurality of third regions of said opposite conductivity type contiguous with said first region to form therewith a respective plurality of P-N junctions each extending to said surface and there defining an enclosed area surrounded by said first enclosed area, and ohmic contacts to said first, second and third regions.

2. A semiconductor device comprising an integral or integrated body of single crystal semiconductor material containing therein or thereon discrete regions adapted to provide the electrical properties of a multi-emitter transistor and one or more other circuit elements, said multi-emitter transistor including a first region of one conductivity type forming a part of one surface of said body, a second region of opposite conductivity type contiguous with said first region to form therewith a first P-N junction extending to said surface and there defining a first enclosed area, a plurality of third regions of said opposite conductivity type contiguous with said first region to form therewith a respective plurality of P-N junctions each extending to said surface and there defining an enclosed area surrounded by said first enclosed area, and ohmic contacts to said first, second and third regions.

3. A semiconductor device according to claim 2, wherein said other circuit element or one of said other circuit elements is a re-

standing of the principles of the invention and various forms and embodiments thereof.

With reference to Fig. 3, there is illustrated a multi-emitter transistor which may be part of a semiconductor body containing other circuit elements as illustrated in Figs. 1 to 2C and described in detail in said parent patent application.

The body of semiconductor material is of single crystal structure and can be composed of any suitable semiconductor material such as germanium, silicon, intermetallic alloys such as gallium arsenide, aluminum antimonide, indium antimonide, as well as others.

The multi-emitter transistor TR2 includes an N-type region 18 provided in the wafer 12, a P-type base region 20 and two N-type emitter regions 22 and 24. Ohmic contacts 26, 28 and 30 may be plated or evaporated onto their corresponding semiconductor regions. Collector lead 33 may be soldered or alloyed to substrate 10, and extends beneath the left-hand end of wafer 12 and makes ohmic contact therewith. The semiconductor device illustrated in Fig. 3 is a double emitter transistor and provides one NPN transistor plus an integral diode formed by the additional emitter region. The base and emitter regions may be formed by selective diffusion into the wafer 12.

The transistor TR3 illustrated in Fig. 1 is identical with TR2 illustrated in Fig. 3.

The multi-emitter transistor, Fig. 3, may have its collector region 18 mounted or secured to a substrate 10 which substrate may be intrinsic semiconductor material having a relatively high order of resistivity or the entire unit could be formed from a block of intrinsic semiconductor material into which doping impurities are diffused in the region occupied by the collector. According to the latter arrangement, the substrate 10 would be part of the same physical piece of semiconductor material as collector 18 and differing therefrom only in its electrical characteristics due to the impurity doping.

The multi-emitter transistor illustrated in Fig. 3 may be integrated with other circuit elements in a body of semiconductor material as described in said parent patent application wherein the manufacture and construction of semiconductor devices illustrated in Figs. 1 to 2C and 4 to 6 are described in detail. The collector-base P-N junction extends to one surface of the body and there defines an enclosed area and each emitter-base P-N junction extends to said one surface and there defines another enclosed area surrounded by said first-mentioned enclosed area. Therefore, the multi-emitter transistor illustrated in Fig. 3 may be combined with other circuit elements such as multi-emitter transistor TR3, diffused resistors R1 and R3, capacitors C1 and C2, diodes D2 and D3, and transistor TR1.

It must be emphasized that only several embodiments of the invention have been described and that other variations and modifications thereof may be made without departing from the scope of the invention which is defined in the appended claims.

Reference is additionally made to our copending patent applications nos. 23279/63; 46087/63; 46088/63; 46089/63; and 46090/63, (Serial nos. 958244, 958246, 958247, 958248 and 958249), also divided from said parent application no. 16071/60 with(Serial no. 958242).

Terms indicative of position, such as "thereon", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilised in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising an integral or integrated body of single crystal semiconductor material containing therein or thereon a first region of one conductivity type forming a part of one surface of said body, a second region of opposite conductivity type contiguous with said first region to form therewith a first P-N junction extending to said surface and there defining a first enclosed area within the periphery of said surface, a plurality of third regions of said opposite conductivity type contiguous with said first region to form therewith a respective plurality of P-N junctions each extending to said surface and there defining an enclosed area surrounded by said first enclosed area, and ohmic contacts to said first, second and third regions.

2. A semiconductor device comprising an integral or integrated body of single crystal semiconductor material containing therein or thereon discrete regions adapted to provide the electrical properties of a multi-emitter transistor and one or more other circuit elements, said multi-emitter transistor including a first region of one conductivity type forming a part of one surface of said body, a second region of opposite conductivity type contiguous with said first region to form therewith a first P-N junction extending to said surface and there defining a first enclosed area, a plurality of third regioins of said opposite conductivity type contiguous with said first region to form therewith a respective plurality of P-N junctions each extending to said surface and there defining an enclosed area surrounded by said first enclosed area, and ohmic contacts to said first, second and third regions.

3. A semiconductor device according to claim 2, wherein said other circuit element or one of said other circuit elements is a re-

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sistor including an elongated portion of semiconductor material bounded by a P-N junction.

4. A semiconductor device according to claim 2, wherein said other circuit element or one of said other circuit elements is a transistor including a fourth region of one conductivity type forming a part of said surface, a fifth region of opposite conductivity type contiguous with said fourth region to form therewith a second P-N junction extending to said surface and there defining a second enclosed area, a sixth region of conductivity type opposite to that of said fourth region and contiguous therewith to form a third P-N junction extending to said surface and there defining a third enclosed area surrounded by said second enclosed area.

5. A semiconductor device according to claim 2, wherein said other circuit element or one of said other circuit elements is a diode including two regions of opposite conductivity types forming therebetween a P-N junction extending to said surface and there defining an enclosed area.

6. A semiconductor device according to claim 4, wherein said transistor is a multi-emitter transistor including a seventh region of conductivity type opposite to that of said fourth region and contiguous therewith to form a fourth P-N junction extending to said surface and there defining a fourth enclosed area surrounded by said second enclosed area.

7. A semiconductor device according to claim 3, wherein said resistor is electrically connected to said second region.

8. A semiconductor device according to claim 4, wherein said second region is electrically connected to said fourth region.

9. A semiconductor device according to claim 3, wherein said resistor is electrically connected to said first region.

10. A semiconductor device according to claim 1, wherein said body includes therein or thereon an elongated portion of semiconductor material bounded by a P-N junction which elongated portion provides the electrical properties of a resistor.

11. A semiconductor device according to claim 1, wherein said body includes a fourth region of one conductivity type forming a part of said surface, a fifth region of opposite conductivity type contiguous with said fourth region to form therewith a second P-N junction extending to said surface and there defining a second enclosed area, and a sixth region of conductivity type opposite to that of said fourth region and contiguous therewith to form a third P-N junction extending to said surface and there defining a third enclosed area surrounded by said second enclosed area, whereby said fourth, fifth and sixth regions provide the electrical properties of a transistor.

12. A semiconductor device according to claim 1, wherein said body includes two regions of opposite conductivity types forming therebetween a P-N junction extending to said surface and there defining an enclosed area, whereby said two regions provide the electrical properties of a diode.

13. A semiconductor device according to claim 11, wherein said transistor is a multi-emitter transistor including a seventh region of conductivity type opposite to that of said fourth region and contiguous therewith to form a fourth P-N junction extending to said surface and there defining a fourth enclosed area surrounded by said second enclosed area.

14. A semiconductor device according to claim 10, wherein said resistor is electrically connected to said second region.

15. A semiconductor device according to claim 11, wherein said second region is electrically connected to said fourth region.

16. A semiconductor device according to claim 10, wherein said resistor is electrically connected to said first region.

17. A semiconductor device according to any preceding claim, including input potentials and/or bias potentials electrically connected to said third regions.

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ERRATA

SPECIFICATION NO. 958,245

Amendment No. 1

Page 2, line 79, *delete* "with" *before* "(serial".

Page 2, line 120/121, *for* "regioins" *read* "regions".

THE PATENT OFFICE,
28th May, 1965