

ABSTRACT

Very High Speed Arbitrary Number of Multiple Signal Multiplexer

5 This invention provides a circuit and a method for very high-speed multiplexers. It provides a circuit that can produce an arbitrary number of multiple signal multiplexers. It also provides a circuit and a method which converts a parallel data bus into a serial data path. This invention contains an overlapped data generator, which takes in a data bus and outputs even and odd
10 signals to a selective mux. It also contains a selective mux, which receives even and odd internal data bits from said overlapped data generator and which outputs one serial data bit. It also contains a phase locked loop/delay locked loop, PLL/DLL, which receives a set of phase clocks and which outputs five evenly-phase-distributed clock signals to a data select signal generator. Finally, the
15 circuit includes a data select signal generator, which receives said five evenly-phase-distributed clock signals and which generates a ten-bit data select signal bus.

Figure 2 is suitable for publication

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