

ABSTRACT

A flash memory device includes: first pads; second pads; third pads; a memory cell array; a row decoder block; a buffer block that stores a command and an address received from an external semiconductor chip through the first pads and provides the address to the row decoder block; a page buffer block that is connected to the memory cell array through bit lines, is connected to the third pads through data lines, and exchanges data signals with the external semiconductor chip through the data lines and the third pads; and a control logic block that receives the command from the buffer block, receives control signals from the external semiconductor chip through the second pads, and controls the row decoder block and the page buffer block based on the received command and the received control signals.

FIG. 4