

CLAIMS

1. A package substrate comprising:
a substrate body comprising a plurality of first contact points on a surface
5 thereof configured for electrical connection to a first die and a plurality of second contact
points on the surface configured for electrical connection to a second die; and
a bridge coupled to the substrate body, the bridge comprising active device circuitry
that is coupled to ones of the plurality of first contact points and ones of the plurality of
second contact points.
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2. The package substrate of claim 1, wherein the bridge is embedded in the substrate
body.
3. The package substrate of claim 2, wherein the active circuitry comprises at least one
15 repeater.
4. The package substrate of claim 3, wherein the at least one repeater is disposed in a
signal path between one of the plurality of first contact points and one of the plurality of
second contact points.
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5. The package substrate of claim 2, wherein the active circuitry comprises control logic.
6. The package substrate of claim 2, wherein the active circuitry comprises a memory
interface.
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7. The package substrate of claim 2, wherein the first plurality of contact points are
operable for connection to a microprocessor and the second plurality of contact points are
operable for connection to at least one memory die and the active circuitry comprises a
memory controller.
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8. The package substrate of claim 2, wherein the bridge comprises at least one passive
signal line coupled to one of the plurality of first contact points and one of the plurality of
second contact points.

9. A package assembly comprising:
a package substrate body comprising a plurality of first contact points on a surface thereof configured for electrical connection to a first die and a plurality of second contact points on the surface configured for electrical connection to a second die;
5 a bridge coupled to the substrate body, the bridge comprising active device circuitry that is coupled to ones of the plurality of first contact points and ones of the plurality of second contact points; and
a first die coupled to the plurality of first contact points and a second die coupled to the plurality of second contact points.
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10. The package assembly of claim 9, wherein the bridge is embedded in the substrate body.
11. The package assembly of claim 10, wherein the active device circuitry is configured
15 to route input/output electrical signals.
12. The package assembly of claim 10, wherein the active circuitry comprises at least one repeater.
- 20 13. The package assembly of claim 12, wherein the at least one repeater is disposed in a signal path between one of the plurality of first contact points and one of the plurality of second contact points.
14. The package assembly of claim 10, wherein the active circuitry comprises control
25 logic.
15. The package assembly of claim 10, wherein the active circuitry comprises a memory circuit.
- 30 16. The package assembly of claim 10, wherein the first die is a microprocessor and the second die is at least one memory die and the active circuitry comprises a memory controller.
17. The package assembly of claim 10, wherein the first die is a microprocessor and the second die is a microprocessor.

18. The package assembly of claim 10, wherein the bridge comprises at least one passive signal line coupled to one of the plurality of first contact points and one of the plurality of second contact points.

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19. A method of forming a package assembly comprising:
coupling a first die to a package substrate, the package substrate comprising a bridge substrate comprising active device circuitry; and
coupling a second die to the package substrate,

10 wherein coupling the first die and the second die to the package substrate comprises coupling the first die and the second die to the active circuitry.

20. The method of claim 19, wherein the active device circuitry comprises a repeater.

15 21. The method of claim 19, wherein the first die is a microprocessor and the second die is at least one memory die and the active circuitry comprises a memory controller.

22. The method of claim 19, wherein the first die is a microprocessor and the second die is a microprocessor.

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