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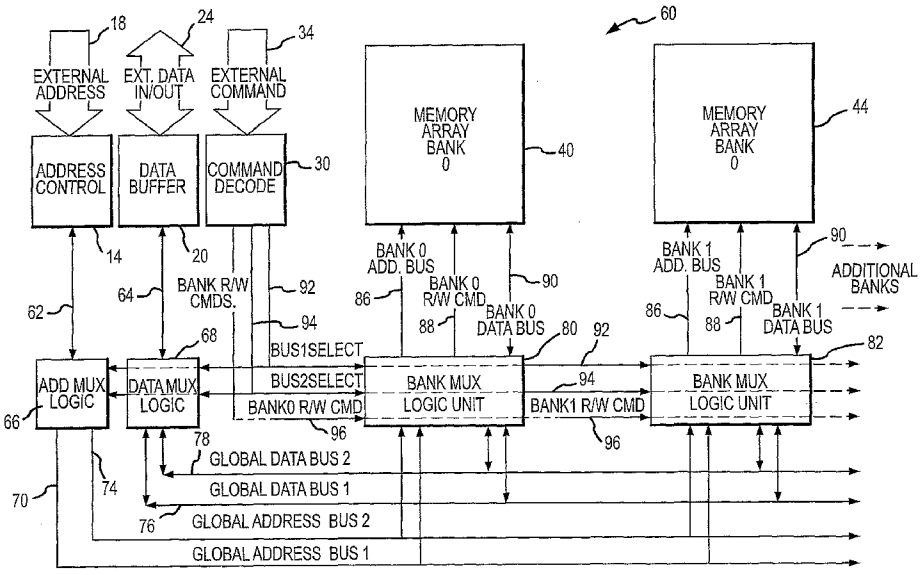
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(54) **Title:** MEMORY DEVICE AND METHOD HAVING MULTIPLE ADDRESS, DATA AND COMMAND BUSES



(57) **Abstract:** A dynamic random access memory ("DRAM") device includes a pair of internal address buses that are selectively coupled to an external address bus by an address multiplexer, and a pair of internal data buses that are selectively coupled to an external data bus by a data multiplexer. The DRAM device also includes a bank multiplexer for each bank of memory cells that selectively couples one of the internal address buses and one of the internal data buses to the respective bank of memory cells. Select signals generated by a command decoder cause the multiplexers to select alternate internal address and data buses responsive to each memory command received by the command decoder.

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