

Claims

1. A light emitting diode structure comprising:
 - a p-type region;
 - an n-type region; and
 - 5 a light emitting region for recombination of carriers injectable by the p-type region and the n-type region, wherein at least one of the n-type region and the p-type region is at least partially formed in a via passing through the light emitting region, wherein the via defines the perimeter of a light emitting surface of at least one pixel.
- 10 2. The light emitting diode structure of claim 1, wherein the light emitting region comprises at least one epitaxial quantum well layer and/or wherein the via enables lateral carrier injection in the light emitting region.
- 15 3. The light emitting diode structure of any preceding claim, wherein both the n-type region and the p-type region are at least partially formed in vias passing through the light emitting region, and/or wherein the light emitting diode structure comprises a further via, wherein the via and the further via are arranged respectively to provide an anode and a cathode.
- 20 4. The light emitting diode structure of any preceding claim, comprising a further light emitting region.
- 25 5. The light emitting diode structure of claim 4, wherein the light emitting region and the further light emitting region are separated by an undoped region thereby to provide a stack of light emitting regions, preferably wherein the via passes through both the light emitting region and the further light emitting region, more preferably wherein the light emitting region and the further light emitting region are configured to emit light of different wavelengths, yet more preferably wherein the light emitting region and the further light emitting region are arranged such that the surface areas of the
- 30 light emitting region and further light emitting region partially overlap, yet more preferably wherein the light emitting diode structure comprises at least three light emitting regions, wherein one of the light emitting regions emits blue light, one of the

light emitting regions emits green light and one of the light emitting regions emits red light.

- 5 6. The light emitting diode structure of any preceding claim, wherein the via is a grid via defining an array comprising a plurality of pixels, preferably wherein the grid is arranged to provide a common electrode, more preferably wherein at least one pixel of the plurality of pixels comprises a further electrode, yet more preferably wherein the further electrode is centrally located within the perimeter of the light emitting surface of at least one pixel, yet more preferably wherein at least two pixels are
- 10 configured to emit light of different wavelengths.
7. The light emitting diode structure of any of claims 4 to 6, wherein the further via comprises a columnar via and at least one of the n-type and p-type region is formed in the further via, preferably wherein the columnar via is arranged to provide an
- 15 electrode thereby to enable control of emission in a pixel defined by the via.
8. The light emitting diode structure of any preceding claim, wherein the light emitting region and/or further light emitting region is formed on an undoped epitaxial layer, and/or wherein the light emitting region and/or further light emitting region is formed
- 20 between undoped epitaxial layers, preferably wherein the undoped epitaxial layer is formed on a barrier layer configured to block vertical carrier diffusion, more preferably wherein the undoped epitaxial layer is gallium nitride, yet more preferably wherein the barrier layer is AlGaIn.
- 25 9. The light emitting diode structure of any preceding claim, wherein at least one of the n-type region and the p-type region is formed in a via that is connected to a planar n-type region or a planar p-type region respectively.
- 30 10. The light emitting diode structure of any preceding claim, wherein the n-type region and/or the p-type region is formed in the via by selected area growth of n-type material and/ p-type material, respectively.

11. The light emitting diode structure of any preceding claim, wherein the via is an etched via.
12. The light emitting diode structure of any preceding claim, wherein the light emitting surface has an area based on the diffusion length of carriers within the light emitting region, preferably wherein the light emitting surface area is less than or equal to $100\mu\text{m}^2$, and more preferably less than or equal to $16\mu\text{m}^2$.
13. The light emitting diode structure of any preceding claim, wherein the at least one pixel is defined peripherally entirely by a single electrode.
14. A high resolution micro LED array comprising the light emitting diode structure of any of claims 1 to 13.
15. The high resolution micro LED array of claim 14, wherein the array is a multi-colour array and/or wherein the array has a pixel pitch less than 10 microns, preferably less than 4 microns.
16. A method of forming a light emitting diode structure comprising:
- a p-type region;
 - an n-type region; and
 - an light emitting region for recombination of carriers injectable by the p-type region and the n-type region, wherein at least one of the n-type region and the p-type region is at least partially formed in a via passing through the light emitting region, wherein the via defines the perimeter of a light emitting surface of at least one pixel.
17. The method of claim 16 wherein the light emitting region comprises at least one epitaxial quantum well layer and/or wherein the via enables lateral carrier injection in the light emitting region, the method preferably comprising forming a plurality of epitaxial layers on a substrate, preferably wherein the plurality of epitaxial layers comprises the n-type region and the light emitting region, more preferably comprising etching through the light emitting region to provide the via defining the pixel

perimeter, preferably comprising growth of the p-type region or n-type region at least partially in the via, more preferably comprising etching a further via for the p-type region or the n-type region.

- 5 18. The method of any of claims 16 or 17, comprising
forming both the n-type region and the p-type region in vias passing through
the light emitting region, preferably comprising providing a further via, wherein the
via and the further via are arranged respectively to provide an anode and a cathode,
more preferably wherein the further via is a columnar via and the n-type or p-type
10 region is formed in the further via, yet more preferably wherein the columnar via is
arranged to provide an electrode thereby to enable control of emission in a pixel
defined by the via.
- 15 19. The method of claim 18, wherein the light emitting region and the further light
emitting region are arranged such that the surface areas of the light emitting region
and further light emitting region partially overlap, preferably wherein the planar
surface area of the further light emitting region is less than the planar surface area of
the light emitting region.
- 20 20. The method of any of claims 18 or 19, comprising at least three light emitting regions,
wherein one of the light emitting regions emits blue light, one of the light emitting
regions emits green light and one of the light emitting regions emits red light.
- 25 21. The method of any of claims 16 to 20, wherein the via is a grid via defining a plurality
of pixels, preferably wherein the grid is arranged to provide a common electrode,
more preferably further comprising forming a further electrode for at least one of the
pixels, yet more preferably wherein the further electrode is formed centrally within
the perimeter of the light emitting surface of the at least one pixel, still more
preferably wherein at least two pixels are configured to emit light of different
30 wavelengths.

22. The method of any of claims 16 to 21, comprising forming the n-type region and/or the p-type region in the via by selected area growth of n-type material and/or p-type material respectively.
- 5 23. The method of any of claims 16 to 21, comprising etching through the light emitting region to form the via, preferably wherein the further via passes through a light emitting region configured to provide a particular wavelength, more preferably comprising etching a yet further via for the p-type region or the n-type region, wherein the further via and the yet further via are arranged to allow carrier injection in
10 different light emitting regions, thereby to provide light of different wavelength, yet more preferably comprising at least partially etching through at least one light emitting region in order locally to remove an unwanted longest wavelength.
24. A method of forming a high resolution LED array comprising any of claims 16 to 23.
- 15 25. The method of claim 24, wherein the array is a multicolour array, preferably wherein the array has a pixel pitch of less than 10 microns, preferably less than 4 microns.
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