

PROCESS FOR READING INFORMATION

The invention relates to a process for reading a record carrier as well as to a device applying such a process.

The invention applies especially to the reading of magnetic or optical recordings and, more particularly, to the reading of high-density recordings. It finds a preferential application in recording systems such as computer peripherals and all business systems.

In a digital recorder, the decoding of the binary information involves regenerating the time reference signal, referred to as the clock signal, which served in the recording of the information. This clock signal is usually produced by a voltage controlled oscillator (VCO) inserted into a phase locked loop (PLL) which is synchronized with the transitions of the reading signal.

In a multi-track recorder, it is possible to use a single clock signal reconstructed for the tracks as a whole, on condition that the synchronization between all the tracks written on the tape is preserved.

This presupposes that the recording heads and reading heads are aligned, and that the tape does not deform. If these conditions are not strictly complied with, the time references of the various tracks become offset one with respect to another, this being the slippage phenomenon known to those skilled in the art as "skew".

In the case in which the binary information is contained on a large number of parallel tracks, for example in the case in which the pitch between parallel tracks is of the order of 10 to 20 μm , it is virtually impossible to maintain this slippage phenomenon within acceptable limits. It is then known to produce an independent clock regeneration circuit for each track. This has numerous drawbacks including, in particular, that of having to produce a large number of circuits.

The invention does not have these drawbacks.

The subject of the present invention is a process for reading binary information written on a carrier and constituting at least one track, the said
5 binary information having been written onto the carrier at the frequency F_{bit} , characterized in that it comprises:

- a step of reading said binary information at the sampling frequency F_e so as to constitute a
10 succession of successive read samples $SAM(k)$ of the same track, k being the index of the read sample $SAM(k)$, each read sample $SAM(k)$ having its phase $\phi(k)$ lying between 0 and 2π ,

- a step of interpolation making it possible to
15 calculate an interpolated sample $I(k)$ with phase equal to π corresponding to the read sample $SAM(k)$, on the basis of the read sample $SAM(k)$ and of the $i + j$ read samples $(SAM(k-i), \dots, SAM(k+j))$ which bracket the read sample $SAM(k)$ such that:

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$$I(k) = a_{k-i} SAM_{(k-i)} + \dots + a_k SAM_{(k)} + \dots + a_{k+j} SAM_{(k+j)},$$

the coefficients $a_{k-i}, \dots, a_k, \dots, a_{k+j}$ having values chosen in accordance with the law of interpolation,

25 - and a step of validation making it possible to generate an information item intended to validate or to invalidate the interpolated sample $I(k)$.

The subject of the present invention is also a system for reading binary information written on a
30 magnetic carrier and constituting at least one track, the said binary information having been written onto the carrier at the frequency F_{bit} , comprising:

- a magneto-optical reading head making it possible to transform into luminous information the
35 binary information read simultaneously on at least one track at the sampling frequency F_e ,

- a charge-transfer photosensitive device gathering the said luminous information and making it possible to transform the said luminous information

into a succession of voltage samples, the said photosensitive device comprising at least one output evacuating the said voltage samples,

characterized in that it comprises:

- 5 - delay means (1, 2) connected to the said output and making it possible to rearrange the gathered voltage samples on the said output in such a way as to obtain a succession of successive read samples SAM(k) of the same track, k being the index of the sample
10 SAM(k) on the track, means of interpolation making it possible to calculate an interpolated sample I(k) for each read sample SAM(k) on the basis of the sample SAM(k) and of the i + j read samples which bracket the sample SAM(k) in such a way that:

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$$I(k) = a_{k-i} \text{ SAM}(k-i) + \dots + a_k \text{ SAM}(k) + \dots + a_{k+j} \text{ SAM}(k+j),$$

- the coefficients $a_{k-i}, \dots, a_k, \dots, a_{k+j}$ having values dependent on the law of interpolation chosen, and means
20 of validation making it possible to generate an information item (VAL) intended to validate or to invalidate the interpolated sample I(k).

An advantage of the invention is that it avoids multiplication of the clock regeneration circuits and
25 binary information decoding circuits.

Other characteristics and advantages of the invention will emerge on reading a preferred embodiment given with reference to the appended figures in which:

- Figure 1 represents an example of a
30 recording/reading system to which the invention applies;

- Figure 2 represents a schematic block diagram of the device of the invention;

- Figure 3 represents a schematic diagram of
35 the interpolator (INT) represented in Figure 2;

- Figure 4 represents a schematic diagram of the sort operator (SRT) represented in Figure 2;

- Figure 5 represents a first application of the device according to the invention;

- Figure 6 represents a second application of the device according to the invention;

- Figure 7 represents the view on the section A-A of Figure 6 of a first embodiment of the second application;

- Figure 8 represents the view on the section A-A of Figure 6 of a second embodiment of the second application.

In all the figures, the same labels designate the same elements.

Figure 1 represents an example of a recording/reading system to which the invention applies. Recording is carried out with a matrix head and reading with a magneto-optical system. More generally, the invention relates to other recording/reading systems. For these other systems, the carrier on which the information is recorded might not be a magnetic carrier but might be an optical carrier. It may take the form of a disk rather than a tape. Reading can be carried out by any known means other than a light beam, for example by a multitrack head with magneto-resistive elements.

The system described in Figure 1 includes a record carrier such as a magnetic tape MT. A matrix recording head MH1 includes a matrix of elementary heads MH2 which is controlled by line selection conductors MH3 and data selection conductors MH4. This head makes it possible to record various information tracks t1, t2, ... tX on the tape MT.

Represented on the right in the figure is a magneto-optical reading head RH such as that described in French Patent Application No. 89 17313 filed on 28 November 1989 on behalf of Thomson Consumer Electronics.

This head RH includes a magneto-optical transducer RH1, for example a Kerr-effect transducer, arranged parallel to the plane of the magnetic tape and whose major length is transverse to the length of the tape. A light source RH2 illuminates, by a beam of

polarized light and through a focusing system RH3, the transducer RH1 in such a way that the light beam is focused substantially as a line on a face of the transducer RH1 in proximity to the magnetic tape MT.

5 The polarization of the beam reflected by the transducer RH1 is modified on the basis of the magnetic field on the tape. The reflected beam is transmitted by a focusing system RH4 and a tracking system RH5 to an opto-electronic detector RH6.

10 Preferably, the detector RH6 is a charge-transfer photosensitive device consisting of a photosensitive zone and of a non-photosensitive zone. The photosensitive zone then preferably consists of a linear array of N_p pixels and the non-photosensitive
15 zone of a read register consisting of transfer stages. The charge generated in a pixel of the photosensitive zone is gathered in a transfer stage of the read register. The detector RH6 comprises at least as many pixels as there are tracks on the tape.

20 The transducer RH1 reflects towards the detector RH6 a beam consisting in reality of a collection of track reading beams each having had its polarization altered by a track of the magnetic tape. This collection of reading beams is received by the
25 detector RH6 which thus makes it possible to detect the information read on each track of the tape MT.

When the tape runs in the direction indicated by arrow FL, the magneto-optical transducer RH1 simultaneously reads the binary information of like
30 index R ($R = 1, 2, \dots, k-1, k, k+1, \dots$) situated on the X parallel tracks $t_1, t_2, \dots, t_X$.

The information read may have been recorded at the same instant. It may also be information recorded in a manner staggered over time. Preferably, the
35 information read is sampled at a frequency F_s greater than the frequency F_{bit} with which it is written on the tape MT.

Figure 2 represents a schematic block diagram of the device of the invention.

For reasons of convenience only the read register RR of the detector RH6 has been represented in Figure 2. The read register RR consists of a succession of N_p transfer stages TS1, TS2, ... , TS N_p . The output
5 circuit OC of the read register consists of a charge/voltage converter comprising a read diode and a first read amplifier which are not represented in the figure.

The signal from the output circuit OC consists
10 of a train of serial information. In a manner known per se, the signal from the output circuit OC passes successively through a second read amplifier RA, an analogue/digital converter ADC, a high-pass filter FI, an equalizer EQ and a corrector CR. The corrector CR is
15 a circuit correcting the crosstalk existing between a pixel and the two neighbouring pixels surrounding this pixel. The corrector CR can be, for example, such as that described in the patent application filed in France on behalf of the Applicants on 22 December 1992
20 and registered as number 92 15474.

As mentioned earlier, the information read simultaneously by the transducer RH1 is the information of like index k contained on the X parallel tracks. The digital operators such as the high-pass filter FI, the
25 equalizer EQ and the corrector CR then possess as many delay circuits as is required for the successive samples which they process to represent the successive information from the same track.

In an analogue transmission channel a phase
30 varying continuously from 0 to 2π is associated with the analogue signal read $x(t)$. Demodulation is generally performed by observing the sign of the signal $x(t)$ at the instant or the phase is equal to π .

In a digital transmission channel, such as that
35 of the invention, the signal read is a string of samples whose phases are discretized. Thus, samples whose phase is equal to π are not necessarily available. The device of the invention consists in calculating by interpolation, for each sample, a new

sample, whose phase is equal to π with the help of the neighbouring samples from the same track. The device according to the invention makes it possible to minimize the probabilities of reading error since, during decoding, the amplitude of the signal detected is calculated at its optimum phase. From this it follows that the invention is particularly advantageous in respect of signals conveyed in high-density or high-throughput channels possessing low signal-to-noise ratios.

The rate of writing the binary information, commonly referred to as bits, contained on the same track defines the frequency F_{bit} . The samples are extracted at the sampling frequency F_e greater than F_{bit} and the ratio of F_e to F_{bit} defines the oversampling factor.

According to the invention, each sample SAM from the corrector CR is sent simultaneously to a phase monitoring circuit DP and to an interpolator INT.

The function of the phase monitoring circuit DP is to estimate the phase ϕ of the sample SAM. The estimated phase information ϕ is sent to the interpolator INT.

The interpolator INT therefore receives the amplitude and the estimated phase of each sample SAM. As will be made precise in Figure 3, the function of the interpolator INT is to calculate by interpolation the value I to be assigned to the sample of index k on the basis of the value of the sample SAM(k) of index k and of values of samples which bracket the sample SAM(k) on the same track.

According to the invention, the interpolator INT also allows the calculation of a validation signal VAL associated with the interpolated sample I and making it possible to validate or invalidate the sample I. The principle of this validation is described in detail in Figure 3.

The interpolated sample I as well as the validation signal VAL which is associated therewith are

then sent to a sort operator SRT whose function is to sort the samples I so as to retain only those which are validated. The signal SI obtained at the output of the operator SRT then consists either of the succession of
5 the validated bits, or consists of the succession of words grouping the validated bits together into packets as described in Figure 4.

Figure 3 represents a schematic block diagram of the interpolator represented in Figure 2.

10 According to the embodiment represented in Figure 3, the interpolation calculation for the sample $I(k)$ of index k is performed with the help of the three sampled values $SAM(k-1)$, $SAM(k)$ and $SAM(k+1)$. More generally, the invention relates, however, to the
15 embodiments for which the calculation of the interpolated sample $I(k)$ is performed with the help of the $i+j+1$ samples $SAM(k-i)$, $SAM(k-(i-1))$, ..., $SAM(k)$, ..., $SAM(k+j)$ where i and j are integers which may or may not be equal.

20 The interpolator of Figure 3 comprises three delay operators 1, 2, 3.

The delay operator 1 contains X samples and enables the sample $SAM(k-1)$ of index k to be restored at its output when it receives the sample $SAM(k+1)$ of
25 index $k+1$ at its input.

Similarly, the delay operator 2 whose input is connected to the output of the delay operator 1, contains X samples and enables the sample $SAM(k-1)$ to be restored at its output when its input receives the
30 sample $SAM(k)$.

According to the preferred embodiment, the interpolated sample $I(k)$ of index k is calculated with the aid of the Lagrange interpolation law. More generally, however, other interpolation laws, based on
35 different optimization criteria may also suit.

According to the embodiment described in Figure 3, the calculated interpolated sample $I(k)$ can be written:

$$I(k) = a_{k-1} SAM(k-1) + a_k SAM(k) + a_{k+1} SAM(k+1).$$

For this purpose, the samples $SAM(k-1)$, $SAM(k)$ and $SAM(k+1)$ are sent to the respective multipliers 7, 8 and 9, which have the function of performing the respective multiplications of $SAM(k-1)$ with a_{k-1} , of
5 $SAM(k)$ with a_k and of $SAM(k+1)$ with a_{k+1} . The results from the three multipliers 7, 8 and 9 are then sent to an adder 10 so as to calculate the interpolated sample $I(k)$.

According to the invention, the values of the
10 coefficient a_{k-1} , a_k and a_{k+1} depend on the interpolation law chosen. Their values are selected on the basis of the value of the phase $\phi(k)$ of the sample of index k .

Within the interpolator, the phase $\phi(k)$ appears at the output of the delay operator 3 when the latter
15 receives the phase $\phi(k+1)$ of the sample of index $k+1$ on its input.

The phase $\phi(k)$ is then sent to the phase segment search operator 4. The value of the phase $\phi(k)$ lies in the interval $[0, 2\pi]$. According to the
20 invention, the interval $[0, 2\pi]$ is divided into N phase segments of width $\frac{2\pi}{N}$. By way of example, N is chosen equal to 8. The invention relates, however, to other values of N preferably chosen to be all the greater the smaller the oversampling factor.

25 The phase $\phi(k)$ belongs to one of the N phase segments. With each phase segment there is associated a collection of three precalculated values for the coefficients a_{k-1} , a_k and a_{k+1} . The phase segment search operator therefore also has the function of assigning
30 to the interpolation calculation for the sample $I(k)$ the values of the coefficients associated with the phase segment to which the phase $\phi(k)$ belongs.

The values of the coefficients a_{k-1} , a_k and a_{k+1} are extracted from a table. This table can be, for
35 example, a memory of PROM type. The interpolation calculation for $I(k)$ is then performed in real time. The samples $SAM(k-1)$, $SAM(k)$ and $SAM(k+1)$ are respectively multiplied, in real time, with the

coefficients a_{k-1} , a_k and a_{k+1} .

According to another embodiment, the multiplications of the samples $SAM(k-1)$, $SAM(k)$ and $SAM(k+1)$ by the respective coefficients a_{k-1} , a_k and a_{k+1} are performed beforehand. For each phase segment each of the possible sample values is then multiplied beforehand with each of the coefficients a_{k-1} , a_k and a_{k+1} . According to this embodiment, the values of the samples as well as the values of the phases are what allow the addressing to the adder 10 of the results calculated beforehand.

According to the embodiments just described, the sample $I(k)$ is calculated from 3 sampled values $SAM(k-1)$, $SAM(k)$ and $SAM(k+1)$ and, preferably, the oversampling factor is equal to 2. The invention relates, however, to other embodiments such as, for example, that for which the interpolation is performed on the basis of five successive samples with an oversampling factor equal to 1.5.

The oversampling produces on average N_e samples for N_{bits} bits. The interpolation calculation leads to the calculation of N_e samples $I(k)$. From among the samples $I(k)$ only the N_{bits} to be assigned to the bits need to be retained. It is then necessary for each sample $I(k)$ to be accompanied by an information item enabling it to be validated or invalidated.

This information item, denoted VAL in Figure 4, is generated by the validation operator 6.

The validation operator 6 receives as input the phase $\phi(k)$ of the sample of index k and the phase $\phi(k+1)$ of the sample of index $k+1$. The mean phase difference between two successive samples is equal to

$$2\pi \frac{F_{bit}}{F_e}.$$

It is then possible to define, around the desired phase π , a validation window ranging from $\pi - \pi \frac{F_{bit}}{F_e}$ to $\pi + \pi \frac{F_{bit}}{F_e}$.

The validation operator 6 compares the values

of the phases $\varphi(k)$ and $\varphi(k+1)$ with the upper bound of the validation window, extending the value of $\varphi(k+1)$ onto the segment $[0, 4\pi]$ if necessary.

If the upper bound $\pi + \pi \frac{F_{bit}}{F_e}$ belongs to the
5 interval $[\varphi(k), \varphi(k+1)[$, the information item VAL takes a value signifying that the calculated sample $I(k)$ should be validated.

If the upper bound $\pi + \pi \frac{F_{bit}}{F_e}$ does not belong to
the interval $[\varphi(k), \varphi(k+1)[$, the information item VAL
10 takes a value signifying that the calculated sample $I(k)$ should not be validated.

The comparison constraint relating to a single bound makes it possible to guarantee a validation of a sample even in the presence of changes of tempo of
15 information due, for example, to variations in tape running speed.

The information obtained at the output of the sort operator can consist of the single succession of validated bits. In the case, for example, of the
20 reading of a single track, the sort operator then consists of a memory operating in tempo with the validation signal.

The information obtained at the output of the sort operator can also consist of a succession of words
25 grouping the validated bits together into packets, as described in Figure 4.

To form a word of y bits, y being an integer for example equal to 10, the sort operator SRT then consists of y multiplexers MUX1, MUX2, ..., MUX y , and
30 of y shift registers.

Each multiplexer comprises three poles P1, P2, P3 and a control input C. Under the action of a command applied to C, a link is established either between the poles P1 and P3 or between the poles P2 and P3.

35 Each multiplexer has its poles P3 and P2 connected respectively to the input and to the output of a shift register. Each shift register contains X

stages, X being the number of tracks read. The pole $P1$ of the multiplexer of index 1, $MUX1$, receives the interpolated signal $I(k)$ and the pole $P1$ of the multiplexer of index x greater than 1 ($x = 2, \dots, y$) is connected to the pole $P2$ of the multiplexer of index $x-1$. The outputs of the y shift registers constitute, moreover, a databus B . The control inputs C of all the multiplexers are connected together and to the validation signal VAL .

10 With each clock beat, that is to say in tempo with the sampling frequency F_e , the validation signal is applied simultaneously to all the commands C of the multiplexers. When the signal VAL is required to validate the sample $I(k)$, a link is established between
15 the poles $P1$ and $P3$ of each multiplexer. It follows that the validated sample $I(k)$ enters the shift register of index 1, whilst each shift register of index x greater than 1 ($x=2, \dots, y$) receives, on average, on its input the information item emanating
20 from the shift register of index $x-1$. At the conclusion of a number of clock beats equal to y times the oversampling factor, a word of y bits is made up of the information item stored in the y output stages of the y shift registers. A synchronized device for counting the
25 number of bits stored for each track guarantees the completeness of the reconstituted word. This word is then retrieved on the databus B .

 An advantage of the invention is that of working at a frequency which is not the frequency
30 F_{bits} .

 According to the embodiment described in Figure 2, the optoelectronic detector $RH6$ is a charge-transfer device whose read register comprises just a single output circuit.

35 According to other embodiments, however, the read register of the optoelectronic detector $RH6$ can have several outputs. Advantageously, it is then possible to evacuate the charge contained in the read register at a high rate.

Figure 5 represents a first application of the device according to the invention for which the read register comprises two outputs.

According to this first application, the read
5 register is split in a manner known per se into a so-called "even" register and a so-called "odd" register. The even register retrieves the charge accumulated in the pixels of even index of the photosensitive zone and the odd register retrieves the charge accumulated in
10 the pixels of odd index of the photosensitive zone.

Symbolically, this division of the read register into even and odd registers has been represented in Figure 6 by the presence of the two individual outputs Sa and Sb.

15 Each of the signals from the respective outputs Sa and Sb is then transferred into a read chain of the type of that described in Figure 3.

In order to reconstitute the desired information item in its entirety, a device DI makes it
20 possible to rearrange the signals SIa and SIb from the respective sort operators SRTa and SRTb.

Figure 6 represents a second application of the device according to the invention for which the read register comprises a number Q of outputs.

25 The read register RR consists of Q sub-registers ($R_1, R_2, \dots, R_j, \dots, R_Q$) and each sub-register comprises M transfer stages. For reasons of convenience the number M has been chosen, by way of example, equal to 6. The device according to the
30 invention relates, however, to other embodiments where M is any integer which may be different for two different sub-registers. The M transfer stages of each sub-register R_j follow one another in such a way that the charge is transferred from the stage of index 1 to
35 the stage of index M. The read diode of the charge/voltage converter of the sub-register R_j of index j is integrated into the transfer stage of index M of the sub-register R_j . This transfer stage is denoted ESj in Figure 6 and will subsequently be

referred to as the intermediate output stage.

Advantageously, the read register RR is such that the transfer stages of the sub-registers R_j ($j=1, 2, \dots, Q$) follow one another in such a way that the
5 intermediate output stage ES_j of each sub-register R_j adjoins the stage of index 1 of the sub-register R_{j+1} .

The charge/voltage converter of each sub-register R_j consists overall of the read diode contained in the intermediate output stage ES_j and of a
10 first read amplifier A_j which may or may not, in whole or in part, be integrated into the component to which the read register belongs.

As is known to those skilled in the art, a MOS transistor (not represented in the figure) precharges
15 the capacitance of the diode before the arrival of the charge conveyed into the sub-register R_j .

Each of the signals from the amplifiers A_j ($j = 1, 2, \dots, Q$) is then transferred into a read chain of the type of that described in Figure 2. In order to
20 reconstitute the desired information item I_d in its entirety, the signals $SI_1, SI_2, \dots, SI_j, \dots, SI_Q$ from the respective sort operators $SRT_1, SRT_2, \dots, SRT_j, \dots, SRT_Q$ are rearranged in a device DI.

Figure 7 represents the view on the section A-A
25 of Figure 6.

Represented in Figure 7 are a fraction of the sub-register R_j of index j as well as a fraction of the sub-register R_{j+1} of index $j+1$. The represented fraction of the sub-register R_j consists of a transfer
30 stage TS of known type and of the intermediate output stage ES_j . The represented fraction of the sub-register R_{j+1} is a fraction of the transfer stage TS of known type which adjoins the intermediate output stage ES_j .

By way of example, the transfer mode chosen is
35 of the two-phase type. The invention relates, however, to modes of transfer for which the number of phases is greater than two.

The transfer stage TS is formed in a P-doped substrate 1. A N-doped layer 2 covers the substrate 1

so as to constitute a buried channel. As is known to those skilled in the art, in two-phase mode, the N-doped layer 2 consists of a succession of zones alternately doped N^- and N . An N^- doped zone is understood to mean an N doped zone but doped at a lower proportion than an N doped zone. An electrically insulating layer 3 covers the doped layer 2. The electrodes which allow transfer are produced on top of the electrically insulating layer 3.

10 According to the two-phase transfer mode chosen as an example, four electrodes E_1 , E_2 , E_3 , E_4 participate in the transfer of charge in the stage TS.

 In the direction F defined as going from sub-register R_j to sub-register R_{j+1} , the 4 successive electrodes E_1 , E_2 , E_3 and E_4 respectively cover zones doped N^- , N , N^- , N of the buried channel 2. The two electrodes E_1 and E_2 are connected to the same phase Φ_{i1} and the two electrodes E_3 and E_4 are connected to the same phase Φ_{i2} .

20 The phases Φ_{i1} and Φ_{i2} are adjusted in a known manner in order to ensure the transfer of charge from the transfer stage TS of sub-register R_j to the intermediate output stage OS_j of the same sub-register.

 The intermediate output stage OS_j is also formed in the P-doped substrate 1. In the charge transfer direction, the intermediate output stage comprises in succession: two electrodes E_6 and E_7 connected to the same phase Φ_{i1} , an output electrode 4 to which a voltage V_g is applied, a zone 5 doped N^+ and a zone 6 doped P^+ , the zones 5 and 6 being both formed in the substrate 1.

 The read diode is formed by the junction between the N^+ doped zone and the P doped substrate 1.

35 The electrodes E_6 and E_7 are situated on the surface of the electrically insulating layer 3 and respectively cover an N^- doped zone and an N doped zone of the buried channel 2. The electrode 4 is also situated on the surface of the layer 3 and covers an N^- doped zone. The voltage V_g applied to the electrode 4

allows the transfer of charge into the read diode. The P^+ doped zone 6 constitutes an insulation barrier between sub-register R_j and sub-register R_{j+1} . The voltage which appears on the terminals of the read diode is applied to the input of the first read amplifier A_j (not represented in the figure) by way of the conducting connection K_j .

During the transfer of charge from the photosensitive zone to the read register, the intermediate output stage retrieves the charge accumulated in the pixel adjoining it. Advantageously, the transfer of charge to the output amplifier A_j of each sub-register R_j is then performed in idle time.

The N^+ doped zone 5 stretches in the direction perpendicular to the direction of propagation of charge over the whole of the width of the intermediate output stage. It follows that the electric field which makes it possible to accelerate the charge towards the diode is constant. The acceleration of the charge being uniform, it is also transferred uniformly and, hence, more rapidly than in read registers of known type.

Figure 8 represents the view on section A-A of Figure 6 of a second embodiment of the read register.

Like Figure 7, Figure 8 represents a fraction of sub-register R_j of index j as well as a fraction of sub-register R_{j+1} of index $j+1$. The mode of transfer chosen is of the two-phase type, but, as mentioned earlier, the invention also relates to transfer modes for which the number of phases is greater than two.

The transfer stages TS represented in Figure 8 are identical to those represented in Figure 7. The same is true for the intermediate output stage OS_j except as regards the element making it possible to constitute the insulation barrier between sub-register R_j and sub-register R_{j+1} . The insulation barrier is made by an electrode 7 to which a potential V_i is applied. The electrode 7 is situated on the surface of the layer 3 and covers an N^- doped zone.

Advantageously, the use of a photosensitive

device such as that described in Figure 6 makes it possible to provide very high information throughputs. For example, the use of an optoelectronic detector RH6 having 1024 pixels and 32 outputs and used to read a
5 tape with 1000 tracks provides an information throughput of the order of several hundred Mbits per second.

CLAIMS

1. Process for reading binary information written on a carrier and constituting at least one track, the said binary information having been written onto the carrier at the frequency F_{bit} , characterized in that it comprises a step of reading said binary information at the sampling frequency F_e so as to constitute a succession of successive read samples $SAM(k)$ of the same track, $SAM(k)$ being the read sample of order k , each read sample of order k having its phase $\phi(k)$ lying between 0 and 2π , a step of interpolation making it possible to calculate an interpolated sample $I(k)$ with phase equal to π corresponding to the read sample $SAM(k)$, on the basis of the read sample $SAM(k)$ and of the $i + j$ read samples ($SAM(k-i)$, ..., $SAM(k+j)$) which bracket the read sample $SAM(k)$ such that:

$$I(k) = a_{k-i} SAM(k-i) + \dots + a_k SAM(k) + \dots + a_{k+j} SAM(k+j),$$

the coefficient a_{k-i} , ..., a_k , ..., a_{k+j} having values dependent on the law of interpolation chosen, and a step of validation making it possible to generate an information item (VAL) intended to validate or to invalidate the interpolated sample $I(k)$.

2. Reading process according to Claim 1, characterized in that the validation step consists in comparing the quantity $\pi + \pi \frac{F_{bit}}{F_e}$ with the interval $[\phi(k), \phi(k+1)[$ in such a way that the said information item (VAL) makes it possible to validate the interpolated sample $I(k)$ if $\pi + \pi \frac{F_{bit}}{F_e}$ belongs to the said interval or to not validate the interpolated sample $I(k)$ if $\pi + \pi \frac{F_{bit}}{F_e}$ does not belong to the said interval.

3. Reading process according to either one of Claims 1 or 2, characterized in that the values of the



coefficients $a_{k-i}, \dots, a_k, \dots, a_{k+j}$ are included in tables and are selected on the basis of the value of the phase $\phi(k)$ of the sample $SAM(k)$.

4. Reading process according to Claim 3, characterized in that the values of the said coefficients are precalculated for N phase segments which divide the interval $[0, 2\pi]$ and in that the values chosen for the said coefficients are those corresponding to the phase interval to which the phase $\phi(k)$ of the sample $SAM(k)$ belongs.

5. Reading process according to either one of Claims 1 or 2, characterized in that the values which may be taken by the magnitudes $a_{k-i} SAM(k-i), \dots, a_k SAM(k), \dots, a_{k+j} SAM(k+j)$ are precalculated for N phase segments which divide the interval $[0, 2\pi]$, the values of the samples $SAM(k-i), \dots, SAM(k), \dots, SAM(k+j)$ being taken from among all the values which may be taken by the said samples, and in that the values chosen for the said magnitudes are those corresponding to the value of the sample $SAM(k)$ and to the phase interval to which the phase $\phi(k)$ of the sample $SAM(k)$ belongs.

6. Reading process according to any one of the preceding claims, characterized in that it comprises a step of sorting the interpolated samples according to whether the said interpolated samples are to be validated or not validated.

7. Reading process according to Claim 6, characterized in that the sorting step makes it possible to group the validated interpolated samples together into packets so as to constitute a succession of words.

8. Reading process according to Claim 6, characterized in that it relates to the reading of a single track and in that the sorting step consists in storing the interpolated samples in tempo with the information item (VAL) intended to validate the interpolated samples.

9. System for reading binary information written



on a magnetic carrier and constituting at least one track, the said binary information having been written onto the carrier at the frequency F_{bit} , comprising:

- reading means making it possible to read the said binary information at a sampling frequency F_e , in such a way as to obtain a succession of successive read samples $SAM(k)$ of the same track, k being the index of the sample $SAM(k)$ on the track;

- means of interpolation making it possible to calculate an interpolated sample $I(k)$ for each read sample $SAM(k)$ on the basis of the sample $SAM(k)$ and of the $i + j$ read samples which bracket the sample $SAM(k)$ in such a way that:

$$I(k) = a_{k-i} SAM(k-i) + \dots + a_k SAM(k) + \dots + a_{k+j} SAM(k+j)$$

the coefficients $a_{k-i}, \dots, a_k, \dots, a_{k+j}$ having values dependent on the law of interpolation chosen, and means of validation making it possible to generate an information item (VAL) intended to validate or to invalidate the interpolated sample $I(k)$.

10. System for reading binary information written on a magnetic carrier and constituting at least one track, the said binary information having been written onto the carrier at the frequency F_{bit} , comprising:

- a magneto-optical reading head making it possible to transform into luminous information the binary information read simultaneously on at least one track at the sampling frequency F_e ,

- a charge-transfer photosensitive device gathering the said luminous information and making it possible to transform the said luminous information into a succession of voltage samples, the said photosensitive device comprising at least one output evacuating the said voltage samples,

characterized in that it comprises:

- delay means (1, 2) connected to the said output and making it possible to rearrange the gathered voltage samples on the said output in such a way as to



obtain a succession of successive read samples SAM(k) of the same track, k being the index of the sample SAM(k) on the track, means of interpolation making it possible to calculate an interpolated sample I(k) for
5 each read sample SAM(k) on the basis of the sample SAM(k) and of the i + j read samples which bracket the sample SAM(k) in such a way that:

$$I(k) = a_{k-i} \text{ SAM}(k-i) + \dots + a_k \text{ SAM}(k) + \dots + a_{k+j} \text{ SAM}(k+j),$$

10

the coefficients $a_{k-i}, \dots, a_k, \dots, a_{k+j}$ having values dependent on the law of interpolation chosen, and means of validation making it possible to generate an information item (VAL) intended to validate or to
15 invalidate the interpolated sample I(k).

11. System for reading binary information according to one of Claims 9 or 10, characterized in that the interpolation means consist of i+j+1 multipliers (7, 8, 9), each multiplier having a first input and a second
20 input, and of an adder (10), the i+j+1 successive samples SAM (k-i), ..., SAM(k), ..., SAM (k+j) being respectively applied to the first input of the i+j+1 multipliers (7, 8, 9), the second inputs of the said multipliers receiving the respective coefficients $a_{k-i},$
25 ..., $a_k, \dots, a_{k+j}$, the result emanating from each multiplier being sent to the adder (10) so as to obtain the interpolated sample I(k), and in that the validation means consist of a validation operator (6) to which the phase $\varphi(k)$ of the read sample SAM(k) and
30 the phase $\varphi(k+1)$ of the read sample SAM(k+1) are sent in such a way that if the quantity $\pi + \pi \frac{F_{\text{bit}}}{F_c}$ belongs to the interval $[\varphi(k), \varphi(k+1)[$, the said validation operator generates a signal (VAL) making it possible to validate the interpolated sample and if the quantity
35 $\pi + \pi \frac{F_{\text{bit}}}{F_c}$ does not belong to the said interval, the said validation operator generates a signal making it possible to not validate the interpolated sample.



12. Reading system according to any one of Claims 9, 10 or 11, characterized in that it comprises a sort operator (SORT) making it possible to retain only the validated interpolated samples.

5 13. Reading system according to any one of Claims 10 to 12, characterized in that the charge-transfer photosensitive device consists of a photosensitive zone consisting of a linear array of pixels and of a non-photosensitive zone consisting of a read register (RR)
10 consisting of transfer stages, the charge generated in a pixel being gathered in a transfer stage of the read register, the read register (RR) consisting of Q sub-registers (R1, R2, ... Rj, ... , RQ), each sub-register Rj comprising M transfer stages, M being any integer
15 which may be different for two different sub-registers, the M transfer stages of each sub-register following one another in such a way that the charge is transferred from the stage of index 1 to the stage of index M, the transfer stage of index M of each sub-
20 register comprising a read diode making it possible to convert variations in charge which it detects into voltage variations, each read diode of each sub-register constituting an output of the read register (RR).

25 14. Reading system according to either of Claims 9 or 10, characterized in that the magnetic carrier includes several non-synchronously readable information tracks.

30 15. Reading process according to Claim 1, characterized in that the magnetic carrier includes several non-synchronously readable information tracks.

