WHAT IS CLAIMED IS:

1. A vertical memory device comprising:

a channel on a substrate, the channel extending in a vertical direction that is perpendicular to an upper surface of the substrate;

a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern, and a first blocking pattern that are sequentially stacked in a horizontal direction, the horizontal direction parallel to the upper surface of the substrate; and

gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure,

wherein the charge storage structure includes charge trapping patterns spaced apart from each other in the vertical direction, each of the charge trapping patterns facing one of the gate electrodes in the horizontal direction, and

wherein a first length in the vertical direction of an inner sidewall of at least one of the charge trapping patterns facing the tunnel insulation pattern is less than a second length in the vertical direction of an outer sidewall of a respective at least one of the charge trapping patterns facing the first blocking pattern,

wherein the first length of the at least one of the charge trapping patterns is greater than a third length in the vertical direction of a respective one of the gate electrodes.

2. The vertical memory device of claim 1, wherein the first length of each of the charge trapping patterns is greater than the third length in the vertical direction of a respective one of the gate electrodes.

3. The vertical memory device of claim 1 or claim 2, wherein an absolute value of

a slope of an upper surface of each of the charge trapping patterns with respect to the upper surface of the substrate gradually decreases from the tunnel insulation pattern toward the first blocking pattern.

4. The vertical memory device of any one of claims 1 to 3, wherein the charge storage structure further includes a division pattern between ones of the charge trapping patterns neighboring in the vertical direction and contacting the tunnel insulation pattern and the first blocking pattern, and wherein the division pattern includes silicon oxide.

5. The vertical memory device of claim 4, wherein an absolute value of a slope of an upper surface of the division pattern with respect to the upper surface of the substrate gradually decreases from the tunnel insulation pattern toward the first blocking pattern.

6. The vertical memory device of any one of claims 1 to 5, wherein each of the tunnel insulation pattern and the first blocking pattern extends in the vertical direction, and the charge trapping patterns are between the tunnel insulation pattern and the first blocking pattern.

7. The vertical memory device of any one of claims 1 to 6, wherein the charge trapping patterns include silicon nitride, and each of the tunnel insulation pattern and the first blocking pattern includes silicon oxide.

8. The vertical memory device of any one of claims 1 to 7, further comprising:

a second blocking pattern covering lower surfaces, upper surfaces, and a sidewall of each of the gate electrodes, the second blocking pattern including a metal oxide, the sidewall facing the charge storage structure in the horizontal direction.

9. The vertical memory device of any one of claims 1 to 8, wherein the gate electrodes include second and third gate electrodes configured to serve as a word line and an SSL, respectively, and

wherein the vertical memory device further includes,

a semiconductor pattern on the substrate, the semiconductor pattern contacting bottom surfaces of the channel and the charge storage structure, and

a first gate electrode under the second gate electrode on the substrate, the first gate electrode surrounding the semiconductor pattern and configured to serve as a GSL.

10. A vertical memory device comprising:

a channel on a substrate, the channel extending in a vertical direction that is perpendicular to an upper surface of the substrate;

a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern structure, and a blocking pattern that are sequentially stacked in a horizontal direction parallel to the upper surface of the substrate; and

gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure,

wherein the charge storage structure includes charge trapping pattern structures spaced apart from each other in the vertical direction, each of the charge trapping pattern structures facing a corresponding one of the gate electrodes in the horizontal direction, and

wherein each of the charge trapping pattern structures includes first and second charge trapping patterns that are sequentially stacked in the horizontal direction on an outer sidewall

of the tunnel insulation pattern, the first and second trapping patterns including different materials from each other,

wherein a length in the vertical direction of the second charge trapping pattern is greater than a length in the vertical direction of the corresponding one of the gate electrodes.

11. The vertical memory device of claim 10, wherein the first charge trapping pattern includes at least one of silicon carbonitride, silicon boronitride, silicon, or silicon doped with at least one of nitrogen or carbon, and the second charge trapping pattern includes silicon nitride.

12. The vertical memory device of claim 10 or claim 11, wherein a length in the vertical direction of the first charge trapping pattern gradually decreases from the tunnel insulation pattern toward the second charge trapping pattern.

13. The vertical memory device of any one of claims 10 to 12, wherein the second charge trapping pattern covers an outer sidewall and lower and upper surfaces of the first charge trapping pattern.

14. The vertical memory device of claim 13, wherein the second charge trapping pattern includes a first portion covering the outer sidewall of the first charge trapping pattern and contacts the blocking pattern, and a second portion extending from the first portion toward the tunnel insulation pattern to cover the upper and lower surfaces of the first charge trapping pattern.

15. The vertical memory device of any one of claims 10 to 14, wherein the blocking

pattern extends in the vertical direction, and covers an outer sidewall and lower and upper surfaces of the second charge trapping patterns.

16. A vertical memory device comprising:

a channel on a substrate, the channel extending in a vertical direction perpendicular to an upper surface of the substrate;

a charge storage structure on an outer sidewall of the channel, the charge storage structure including a tunnel insulation pattern, a charge trapping pattern, and a blocking pattern that are sequentially stacked in a horizontal direction parallel to the upper surface of the substrate;

a dummy charge storage structure spaced apart from the charge storage structure in the vertical direction on the substrate, the dummy charge storage structure including a dummy tunnel insulation pattern, a dummy charge trapping pattern, and a dummy blocking pattern that are sequentially stacked; and

gate electrodes spaced apart from each other in the vertical direction, each of the gate electrodes surrounding the charge storage structure,

wherein the charge storage structure includes charge trapping patterns spaced apart from each other in the vertical direction, each of the charge trapping patterns facing a corresponding one of the gate electrodes in the horizontal direction, and

wherein the dummy tunnel insulation pattern and the dummy blocking pattern include materials substantially the same as those of the tunnel insulation pattern and the blocking pattern, respectively, and the dummy charge trapping pattern includes a material different from that of the charge trapping patterns,

wherein a length in the vertical direction of each of the charge trapping patterns is greater than a length in the vertical direction of the corresponding one of the gate electrodes.

17. The vertical memory device of claim 16, wherein each of the charge trapping patterns includes silicon nitride, and the dummy charge trapping pattern includes at least one of silicon carbonitride, silicon boronitride, silicon, or silicon doped with at least one of nitrogen or carbon.

18. The vertical memory device of claim 16, wherein

each of the charge trapping patterns includes first and second charge trapping patterns sequentially stacked from the tunnel insulation pattern in the horizontal direction, and

the first charge trapping pattern includes a material substantially the same as that of the dummy charge trapping pattern, and the second charge trapping pattern includes a material different from that of the dummy charge trapping pattern.

19. The vertical memory device of any one of claims 16 to 18, wherein a length in the vertical direction of an inner sidewall of each of the charge trapping patterns contacting the tunnel insulation pattern is less than a length in the vertical direction of an outer sidewall of each of the charge trapping patterns contacting the blocking pattern.

20. The vertical memory device of any one of claims 16 to 19, further comprising:

a division pattern between ones of the charge trapping patterns that neighbor in the vertical direction, the division pattern contacting the tunnel insulation pattern and the blocking pattern and including silicon oxide.