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(54) READ-ONLY MEMORIES

(71) We, TELETYPE CORPORATION of 5555 Touhy Avenue, Skokie, Cook County, State of Illinois, United States of America, a Corporation organised and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to read-only memory arrays.

Read-only memories are employed as components in digital data processing systems. Predetermined information is stored in a read-only memory for use in the data processing system. The information stored in the memory is typically accessed by a binary coded signal which is internally generated by the data processing system normally as an intermediate result in a data processing sequence.

Information is often represented in a read-only memory by the presence and absence of electrical devices at predetermined memory locations. To minimize the number of access leads required to access all the information stored in the memory, the memory locations are arranged in a matrix of columns and rows.

The binary coded access signal is therefore broken down into two parts, one part for accessing columns and the other for accessing rows. For each intersection of a column and a row, a unique information bit is obtained. In most memories the two parts of the digital access signal are next passed through a pair of code translating circuits to provide column and row selection signals. For an example of a code translating circuit see U.S. patent No. 3,631,465.

When read-only memories are fabricated by integrated circuit techniques, the devices employed in the memory can be organized in a compact arrangement thereby efficiently utilizing the available space for active com-

ponents. The code translating circuits on the other hand are not normally as simple or symmetrical as the memory array, therefore, an undue amount of chip area is consumed by the code translating circuits.

The invention provides a read-only memory array in which accessing circuitry is included in the memory array.

According to the invention a memory array comprises intersecting pluralities of row and column conductors and a plurality of variable impedance devices whose impedance state will change when a predetermined switching signal is applied and which are present at predetermined intersections of the row and column conductors, the presence/absence pattern of said impedance devices at intersections associated with a first group of the column conductors representing information stored, and the presence/absence pattern of said impedance devices at intersections associated with a second group of the column conductors resulting in a corresponding different one only of the row conductors having those of its impedance devices associated with said second group of column conductors all in their unchanged impedance states in response to a respective one of different predetermined patterns of said predetermined signals each said impedance device having a control electrode connected to the corresponding column conductor and two other electrodes connected in a distinct path between adjacent row conductors, the signal level applied to the control electrode of a said impedance device determining the impedance between the two other electrodes thereof.

Such an array may be used with means for causing a said predetermined signal to be applied to any desired one of the first group of column conductors.

Suitable output means may provide a first level output signal in response to unchanged impedance states existing for all the impedance devices connected to any one of the row

conductors, and a second level output signal in response to all of the row conductors having at least one of the impedance devices connected thereto in its changed impedance state.

Alternatively, the memory array may be adapted so that a reference voltage applied to the first row conductor will cause to appear at the last row conductor an output signal which is dependent upon whether or not at least one said distinct path between adjacent row conductors is in its changed impedance state.

Embodiments of the invention will now be described, by way of example with reference to the accompanying drawings, in which:

FIG. 1 is a schematic circuit diagram of a portion of a memory constructed in accordance with the principles of this invention particularly showing the memory matrix portion thereof.

FIG. 2 is a circuit diagram of an X decoder circuit used in a memory circuit of this invention.

FIG. 3 is a block diagram showing how to combine FIGS. 1 and 2 to show a read-only memory in accordance with the teachings of this invention.

FIG. 4 is a timing diagram showing clock signals employed to drive the memory circuit of FIG. 3.

FIG. 5 shows partially in schematic and partially in block diagram form, a second memory constructed in accordance with the teachings of this invention.

FIG. 6 is a truth table for an X decoder employed in a memory as taught by this invention.

FIG. 7 is a truth table for the Y decoding function performed integral to the memory array in accordance with teachings of this invention.

In a read-only memory, digitally coded information signals are employed to access permanently stored data. With FIGS. 1 and 2 taken together as shown in FIG. 3, a simplified read-only memory is illustrated in which 16 stored data bits can be accessed by a 4-bit word. The memory array can be looked upon as having five major portions: input circuitry including phase splitters 10-13, an X decoding circuit 14, a matrix 16 having a Y decoding section 17 and a storage section 18, and an output circuit 19. It should be noted that in the memory portion shown in FIG. 1, the storage section 18 and the Y decoding section 17 are physically integral.

Each of the five major portions of the read-only memory may be dynamic logic and/or static (DC) logic circuits. The illustrated matrix 16, which comprises both the storage section 18 and the Y decoding section 17, includes four dynamic logic circuits. Each row of the matrix 16 (terminating at output terminals Y_1 , Y_2 , Y_3 , and Y_4 , respectively), is

formed by a separate dynamic logic circuit. Field effect transistors 21, 22, 23, and 24 are connected one in each row of the matrix 16 and, being P-channel enhancement mode devices, serve as gating transistors to pre-charge capacitors 26, 27, 28, and 29, (representing distributed capacitance), respectively, when a negative signal is applied to a lead 30 interconnecting the gates and the drains of all the field effect transistors 21, 22, 23, and 24. The remaining field effect transistors in each row of the matrix 16, also being P-channel enhancement mode devices, serve as a logic network for the respective gating field effect transistor in that row.

When the signal on the lead 30 is brought to ground level, the field effect transistors 21, 22, 23, and 24 are brought to a high impedance condition leaving the capacitors 26, 27, 28, and 29 negatively charged. If any one of the remaining field effect transistors in a particular row has a negative signal on the gate thereof (indicating specific data conditions as will be explained herein after), the respective capacitors 26, 27, 28, or 29 in that row will be discharged through that field effect transistor to the ground level now appearing on lead 30.

The signals applied to the gates of the various field effect transistors in the matrix 16 are generated in accordance with the received data word, in the example a 4-bit binary word, the individual bits of which appear on corresponding input terminals I_1 , I_2 , I_3 , and I_4 . Two of the signals, I_1 and I_2 , are applied to the phase splitters 10 and 11, which may be of the type disclosed in the last mentioned copending application, providing

output signals on leads I_{s1} , I_{s2} , I_{s3} , each of which is applied to all the field effect transistors in one corresponding column of the matrix 16. The remaining signals I_3 and I_4 are similarly applied to the phase splitters 12 and 13 providing output signals on leads

I_{s3} , I_{s4} , I_{s5} , and I_{s6} , each of which is applied to a group of field effect transistors in the X decoding circuitry 14.

The output signals appearing on leads I_{s1} , I_{s2} , I_{s3} , and I_{s4} are similar to the input signals appearing on leads I_1 , I_2 , I_3 , and I_4 .

The signals appearing on leads I_{s1} , I_{s2} , I_{s3} , I_{s4} are essentially inversions of the signals applied to the phase splitters 10, 11, 12, and 13. Therefore, it should be clear that the function performed by the phase splitters 10, 11, 12, and 13 could also be performed by a simple inverting amplifier.

The X decoding circuitry 14 shown particularly in FIG. 2, together with phase splitters 12 and 13 translates the two bits I_3 and I_4 of the binary coded received data word into a

distinctive "one out of four" signal on a corresponding one of four leads X_1 , X_2 , X_3 , and X_4 to access one and only one column in the storage section 18 of the matrix 16 for each combination of digital signals applied to the input terminals I_3 and I_4 . The truth table for the X decoding circuitry 14 is shown in FIG. 6.

In operation a negative voltage is applied to an input terminal ϕ_2 of the X decoding circuitry 14, bringing the gates and drains of a set of four gating field effect transistors 31, 32, 33, and 34 to a negative potential. This negative potential charges a capacitor 36 through field effect transistor 31, capacitor 37 through field effect transistor 32, capacitor 38 through field effect transistor 33, and capacitor 39 through field effect transistor 34, all capacitors thus being precharged to the negative potential on the input terminal ϕ_2 .

After a predetermined pre-charge interval, the terminal ϕ_2 is brought to ground bringing the gating transistors 31, 32, 33, and 34 to a high impedance condition and preventing discharge of the capacitors 36—39 therethrough to grounded terminal ϕ_2 . During a second time interval, the capacitors 36, 37, 38, and 39 will be discharged if any transistor in the X decoding circuitry connected thereto is in a low impedance condition.

Looking now at FIGS. 1, 2, and 6 together, we see for example that if I_3 and I_4 are in a "0" or ground condition, I_{s3} and I_{s4} will be

at ground while I_{s3} and I_{s4} will be at a negative potential. Therefore, X-decoding field effect transistors 41, 42, 43, and 44 whose gates are connected to column leads I_{s3} and

I_{s4} will be in a low impedance condition while the remaining field effect transistors will be in a high impedance condition. Therefore, capacitor 36 is discharged through field effect transistors 41 and 42 in parallel, capacitor 37 is discharged through field effect transistors 43, and capacitor 38 is discharged through field effect transistor 44, all being discharged to the ground appearing on input terminal ϕ_2 during the second time interval. Capacitor 39 is not discharged since the only field effect transistors connected thereto, 46 and 47 are driven at their gates by the ground signals on leads I_{s3} and I_{s4} . Therefore, only lead X, connecting capacitor 39 to the matrix 16 will have a negative potential thereon while the remaining leads X_2 , X_3 , and X_4 connected to capacitors 36, 37, and 38, respectively, will be at ground.

It can be similarly seen that, owing to the pattern of the eight X-decoding transistors 41, 42, etc., for each of the four possible permutations of input signals applied to the input terminals I_3 and I_4 , a negative signal will be

generated on one and only one of the leads X_1 to X_4 , connecting the capacitors 39 to 36, respectively, to the matrix 16 in accordance with the truth table of FIG. 6.

To retrieve an information bit stored in the storage section 18 of the matrix 16, see FIGS. 1, 2, and 4, a four-bit data word is applied by means not shown to input terminals I_1 to I_4 . At time T_1 , see FIG. 4, the phase splitters 10, 11, 12, and 13 are enabled by a signal applied to enabling leads ϕ_1 thereof to pass the applied data word to the leads I_{s1} to I_{s4} and the complement of the applied data word

to the leads I_{s1} to I_{s4} . A timing signal applied by means not shown to input terminal ϕ of the X decoding circuitry 14 pre-charges the capacitors 36, 37, 38, and 39, during the interval from T_0 to T_1 . At time T_2 , the signal on input terminal ϕ_2 goes to ground selecting the X lead to be enabled in accordance with the third and fourth bits of the four-bit data word thereby accessing a single column of the storage portion 18 of the matrix 16. The signal on the lead ϕ_2 can be brought to its negative condition any time prior to T_2 so long as the interval between the appearance of the negative signal and T_2 is sufficient to pre-charge the capacitors 36, 37, 38, and 39.

A timing signal applied by means not shown to the input terminal ϕ_2 of the matrix 16 pre-charges the capacitors 26, 27, 28, and 29 as previously described. At time T_3 , when the signals on the input terminal ϕ_2 returns to ground level, the capacitors 26, 27, 28, and 29 are discharged if any field effect transistor connected thereto is in an ON impedance condition.

The field effect transistors in the Y decoding section 17 of the matrix 16 will be in ON or OFF conditions in accordance with the signals applied to input terminals I_1 and I_2 . The field effect transistors in the storage section 18 of the matrix 16 will be ON or OFF in accordance with the signals generated by the X decoding circuitry 14.

The field effect transistors in the Y decoding section 17 of the matrix 16 are arranged so that, for each of the four permutations of the two signals applied to the input terminals I_1 and I_2 , all but one of the capacitors 26, 27, 28, and 29 are discharged thereby. Since the X decoding circuitry 14 enables only one column in the storage section 18 of the matrix 16, all of the capacitors 26, 27, 28, and 29 will be discharged if a device (transistor) exists in the storage section 18 of the matrix 16 in the column selected by the X decoding circuitry 14 and the row which is not discharged by the field effect transistors in the Y decoding section 17 of the matrix 16. If no device exists at this storage location, the capacitor connected to this "selected" row remains charged.

At time T4 the output circuitry 19 comprising essentially an OR gate is enabled to detect the presence of a negative signal on any of the capacitors 26, 27, 28, and 29. If a negative signal is detected, a "1" is indicated for the position accessed (corresponding to the absence of a transistor at this position) by the four-bit data word on the input terminals I_1 , I_2 , I_3 , and I_4 . If ground appears on all the capacitors 26, 27, 28, and 29, (corresponding to the presence of a transistor at the accessed position) a "0" is indicated. The pattern of transistors (present or absent) is predetermined during manufacture to provide output signals for the particular permutations of input bits desired for each particular function.

The arrangement and operation of the Y decoding portion 17 of the matrix 16 is similar to the X decoding circuitry 14. However, an important difference exists in the fact that the X decoding circuitry 14 presents voltage levels on inputs X_1 to X_4 to matrix 16 while input signals to column conductors of the Y decoding portion 17 of the matrix 16 control impedance conditions within the matrix 16 of which the Y decoding portion 17 is an integral part. FIG. 7 shows the truth table for the selection of rows by the Y decoding circuitry 17 where "1" represents a high impedance condition and "0" a low impedance condition.

It should be noted that the memory described is accessed solely by column conduc-

tors (access columns I_{a1} , I_{a2} , etc. and memory memory columns X_1 , X_2 , etc.) rather than by column and row conductors. This arrangement is particularly useful when buildings integrated circuit memories because the regular arrangement of the matrix 16 enables the Y decoding function normally performed by additional circuitry to be more compactly included within the matrix 16.

A second memory system embodying the principles of this invention is shown in FIG. 5. A four bit data word applied to input terminals I_1 , I_2 , I_3 , and I_4 actuate phase splitters 10, 11, 12, and 13. The phase splitters 10, 11, 12, and 13 in FIG. 5 are identical to the phase splitters 10, 11, 12, and 13 in the first described embodiment. Static phase splitters or inverters which do not require clocking signals may also be employed in the embodiment shown in FIG. 5. The output signals from the phase splitters 12 and 13 are applied to X decoding circuitry 14 identical to the X decoding circuitry 14 shown in FIG. 2. The X decoding function performed by the X decoding circuitry 14 may also be performed by a static X decoder such as the one described in the first above-mentioned copending application.

The output from the phase splitters 10 and

11 and X decoding circuitry 14 drive column

conductors I_{a1} , I_{a2} , I_{a3} , X_1 , X_2 , X_3 , and X_4 of a memory matrix 48 having a Y decoding section 49 and a storage section 51. Field effect transistors are arranged in columns and rows with gates of field effect transistors being connected to the above-mentioned column conductors while the source and drain of each field effect transistor is connected between adjacent row conductors 52, 53, 54, 56, and 57. With five row conductors, there are four rows of field effect transistors connected therebetween.

A negative potential $-V$ is applied to the uppermost row conductor 52 so that, if at least one field effect transistor in each row is in an ON condition, the negative potential $-V$ will appear on an output terminal 58 directly connected to the row conductor 57.

The field effect transistors in the Y decoding section are arranged to provide an ON impedance in all but one of the rows in accordance with the truth table of FIG. 7. For example, if the four-bit data word applied to the input terminals I_1 , I_2 , I_3 , and I_4 were "0 1 0 1", the first bit applied to phase splitter 10 would provide a "0" on the column conductor I_{a1} and a "1" on the column

conductors I_{a2} thereby actuating field effect transistors 59 and 61. The "1" applied to the input terminal I_2 will actuate phase splitter 11 to provide a "1" on column conductor

I_{a3} and a "0" on column conductor I_{a4} . The "1" on column conductor I_{a3} actuates field effect transistors 62 and 63. Therefore, it is seen that row conductors 52 and 53 are connected by the ON impedance of field effect transistor 63. Row conductors 54 and 56 are connected by the low impedance of the parallel combination of field effect transistors 59 and 62. Row conductors 56 and 57 are connected by the low impedance of field effect transistor 61. Therefore, a high impedance now exists only between row conductors 53 and 54. In this way the Y decoding section 49 of the matrix 48 has selected that row so that a negative signal will appear on the output 58 is the X column lead selected actuates a device connected between row conductors 53 and 54 such as column conductors X_2 . If no device is connected between row conductors 53 and 54 for the column selected by X decoding circuitry 14 such as column conductor X_1 , a ground signal will remain on the output terminal 58.

To complete the example cited above where the input data word is "0 1 0 1", the X decoding circuitry 14 in accordance with the truth table of FIG. 6 will select column conductor X_2 thereby actuating field effect transistor 64 completing the connection

between the voltage $-V$ and the output terminal 58.

A field effect transistor 66 is connected between the output terminal 58 and ground to be driven from a pulse source not shown for discharging stray capacity represented by capacitor 67 before each accessing of the matrix 48. A fixed impedance to ground could replace the field effect transistor 66. The fixed impedance should have a value high compared to the ON impedance or closed circuit impedance of the matrix 48 and now compared with the OFF impedance or open circuit impedance of the matrix 48.

15 WHAT WE CLAIM IS:—

1. A memory array comprising intersecting pluralities of row and column conductors and a plurality of variable impedance devices whose impedance state will change when a predetermined signal is applied and which are present at predetermined intersections of the row and column conductors, the presence/absence pattern of said impedance devices at intersections associated with a first group of the column conductors representing information stored and the presence/absence pattern of said impedance devices at intersections associated with a second group of the column conductors resulting in a corresponding different one only of the row conductors having those of its impedance devices associated with said second group of column conductors all in their unchanged impedance states in response to a respective one of different predetermined patterns of said predetermined signals, each said impedance device having a control electrode connected to the corresponding column conductor and two other electrodes connected in a distinct path between adjacent row conductors, the signal level applied to the control electrode of a said impedance device determining the impedance between the two other electrodes thereof.

2. A memory array according to claim 1,

further comprising means for causing a said predetermined signal to be applied to any desired one of the first group of column conductors.

3. A memory array according to claim 2, further comprising means for providing a first level output signal in response to unchanged impedance states existing for all the impedance devices connected to any one of the row conductors, and a second level output signal in response to all of the row conductors having at least one of the impedance devices connected thereto in its changed impedance state.

4. A memory array according to claim 1 or 2, adapted so that a reference voltage applied to the first row conductor will cause to appear at the last row conductor an output signal which is dependent upon whether or not at least one said distinct path between adjacent row conductors is in its changed impedance state.

5. A memory array according to claim 3 or 4, wherein the means for causing is operative in response to some bit of a multibit data word to energize a first group column conductor according to the values of those bits, and further comprising means responsive to other bits of the same word for applying a pattern of said predetermined signals to the second group column conductors to select a corresponding row conductor thereof according to the values of those other bits.

6. A memory array according to any preceding claim, wherein the impedance devices comprise field effect transistors.

7. A memory array arranged and adapted to operate substantially as herein described with reference to and as shown in FIG. 1, or FIGS 1 and 2 or FIG. 5 of the drawings.

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between the voltage $-V$ and the output terminal 58.

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5. A memory array according to claim 3 or 4, wherein the means for causing is operative in response to some bit of a multibit data word to energize a first group column conductor according to the values of those bits, and further comprising means responsive to other bits of the same word for applying a pattern of said predetermined signals to the second group column conductors to select a corresponding row conductor thereof according to the values of those other bits.

6. A memory array according to any preceding claim, wherein the impedance devices comprise field effect transistors.

7. A memory array arranged and adapted to operate substantially as herein described with reference to and as shown in FIG. 1, or FIGS 1 and 2 or FIG. 5 of the drawings.

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