

A METHOD & APPARATUS FOR DETECTING BACK ELECTROMOTIVE FORCE

Field of the Invention

This invention relates to the detection of back electromotive force (BEMF) in a three-phase brushless DC motor driven by a three-phase Half-Bridge driver and operating in a continuous pulse width modulated (PWM) mode. The invention provides for detection of back electromotive force zero-crossings for use in motor speed control.

Background Art

The spindle motor commonly used in computer hard disk drives (HDD) uses a three-phase drive current drive from a DC power supply. The three-phase sequencing is done by on/off sequencing of the power transistors connected in three-phase half-bridge configuration.

In a typical bipolar operation, at any instant, only two phases are conducting while the third phase is in a tri-stated condition. The voltage monitored in this tri-stated phase is the BEMF voltage. When this BEMF voltage changes its polarity with respect to the centre tap voltage (neutral/star terminal of the motor windings), a zero-crossing is detected. This provides an indication for the next phase advancement and the rate of zero-crossing occurrences is directly proportional to the motor speed. Consequently, BEMF zero-crossing information is important for speed control.

Figure 1 shows the three output voltage waveforms from a typical spindle motor been driven without PWM chopping (linear operation). In this situation, BEMF detection is relatively straight forward.

Figure 2 shows the same waveforms but with PWM chopping. The highly discontinuous waveforms and presence of chopping noise complicates the zero-crossing of the BEMF. Clearly, a simple comparator-latch approach is not adequate as false zero-crossing can

be detected.

In addition, it is a typical system requirement to have one-phase detected BEMF information (say, phase A) as well as "XOR" of the three-phases' detected BEMF. This is usually achieved by BEMF detection for all three-phases through a multiplexing scheme.

To reduce device power dissipation in prior art systems, the spindle motor in a HDD is only driven in PWM mode during start-up when the motor current is high. During run-mode, as the BEMF of the motor increases, the output current decreases and a transconductance loop is used to control the on-resistance of the lower power drivers in a linear fashion for load current (speed) regulation. However, as the disk drive capacity increases, operation at higher motor speeds ($> 7200\text{rpm}$) becomes necessary with a consequential increase in motor running current. This results in higher device power dissipation which can only be reduced by PWM operation during the run-mode of the motor. Unfortunately, this complicates the accurate BEMF detection of BEMF zero-crossings. In one approach, three filters can be used to remove the chopping noises present in the BEMF signal in combination with a comparator with hysteresis. With this approach, the following difficulties arise:

- (1) Since the cut-off frequency is low (max. 1kHz), monolithic filter implementation becomes more complex. Therefore, additional external components are required.
- (2) If the filters are external, the zero-crossing detector must also be external. Alternatively, 3-extra pins are required to keep zero-crossing detection within the chip.
- (3) Highly discontinuous voltage waveforms within the tri-stated phase requires additional BEMF conditioning circuits its to avoid giving false zero-crossing.

Disclosure of the Invention

It is an object of this invention to provide a method and apparatus for detecting the back electromotive force in a three phase brushless DC motor driven in half bridge configuration and operated continuously in a pulse width modulated mode which will overcome or at least ameliorate one or more of the foregoing disadvantages.

According to a first aspect, this invention provides a method of detecting a back electromotive force in a three-phase brushless DC motor driven in half bridge configuration and operated continuously in a pulse width modulated mode, said method comprising the steps of obtaining a difference signal indicative of the difference between the centre tap voltage and the voltage of at least one of said phases during a tri-stated condition of that phase and producing from said difference signal a measure of said back electromotive force.

In a second aspect, this invention provides an apparatus for detecting the back electromotive force in a three-phase brushless DC motor driven in half bridge configuration and operated continuously in a pulse width modulated mode, said apparatus comprising a comparator to produce a difference signal indicative of the difference between the centre tap voltage and the voltage of at least one of said phases during a tri-stated condition of that phase and to produce from said difference signal a measure of said back electromotive force.

Preferably, the signal is obtained during an on cycle of the pulse width modulation. It is further preferred that a reconstructed signal indicative of the back electromotive force is generated from sequential difference signals by holding the reconstructed signal at a hold value determined by each sequential difference signal until the next sequential difference signal is obtained. Preferably, the reconstructed signal is adjusted between sequential difference signals by applying a slope compensation to each hold value. In a preferred embodiment, the slope compensation is achieved by a linear adjustment of the hold value with time. The linear adjustment is preferably determined by a calculation of the rate of change of the back electromotive force at the zero-crossing point for the motor operating speed.

Preferably, the difference signal is obtained following a delay time for the commencement of the on cycle of said pulse width modulation. More preferably, the delay time is about 20% of the pulse width modulation on time.

In the preferred embodiment, a unity-gain fully-differential amplifier is used to compare the difference between the centre tap voltage and the tri-stated phase voltage. This removes common mode noise and the three phase voltages can also be multiplexed.

The differential amplifier output, which is the BEMF signal, is being sampled only during PWM on-time and then held during PWM off time with some appropriate slope compensation to avoid false zero-crossings which can result in speed jitter. Thus, the sample and hold output is a clean replica of BEMF signal and it passes through a BEMF comparator for zero-crossing detection. In addition, in the vicinity of zero-crossing, a window preferably is generated to ensure that there is no PWM off-time, i.e, the full-bridge is in continuous on mode. This avoids losing critical BEMF information at zero-crossings. The comparator output is then latched into the appropriate location. Sample and hold slope compensation can be done easily with prior knowledge of the motor speed and BEMF amplitude.

The method and apparatus of this invention provides for BEMF detection under continuous pulse width mode operation thereby minimising the requirement for power dissipation and permitting higher current motor operation, which in turn, results in a higher motor speed. The invention also eliminates the need for sophisticated filtering techniques to precondition the BEMF waveforms.

The invention will now be described, by way of example only, with reference to the accompanying drawings.

Brief Description of the Drawings

- Figure 1 is a graph of the typical output waveforms for three-phases of a spindle motor used in a hard disk drive in linear operation;
- Figure 2 shows the same waveforms as in Figure 1 with pulse width modulated chopping;
- Figure 3 is a schematic circuit diagram of an embodiment of the present invention;
- Figure 4 respectively shows an actual BEMF signal and a typical sample-and hold BEMF signal.

Figure 5 shows the comparison of the sample and hold signal of Figure 4 with a compensated sample and hold signal according to the present invention.

Figure 6 is a schematic circuit diagram of a circuit which compares a reconstructed BEMF signal with a threshold value; and

Figure 7 shows the use of a small hysteresis in the BEMF voltage.

As shown in Figure 3, a unity gain fully differential amplifier is used to compare the difference between centre tap voltage and the tri-stated phase voltage for each of three-phases A, B and C. A three-channel multiplexer provides for the sequential switching of the phases to the input of the differential amplifier. The multiplexer, which is not shown in detail, has three switches which are conventional in N-channel mos switches. Each switch contains two N-channel LDMOS connected in series with drain-source-source-drain configuration to avoid body diode conduction. The operational amplifier used for the differential amplifier has a low bandwidth (about 1MHz) having push-pull output capable of driving a few milliamperes of current.

Sampling is achieved through a cmos transmission gate containing equal size N-channel and P-channel mos, connected in parallel to avoid switching charge loss. This switch typically offers 50ohm resistance.

The chopping of the power drivers is done by a signal of constant frequency variable duty cycle internal to the device. During high period of the PWM signal both the upper and lower power transistors of the corresponding phases are on and centre tap is approximately at the half of the power supply voltage. During off time one of the outputs goes negative or above power supply due to inductive recirculation and the centre tap voltage changes accordingly. Thus, to have the correct BEMF information, sampling is done during PWM on time. Being an inductive drive with finite core loss, there will be some noise in the centre tap when the chopping is changing from off to on. A delay is incorporated between PWM on time to sampling time. This time is designed to be approximately 20% of the PWM signal's time

period and is externally programmable with a resistor that defines the output slew rate. The PWM frequency is usually set above the audible frequency range, typically 20Khz.

An external capacitor is used as hold capacitor for a sample and hold system. During sampling this capacitor is charged to $(V_{ref} + V_{bemf})$ and during the hold period of the switch it holds the charge, hence the voltage. The typical sample and hold (S/H) output waveform is shown in Figure 4.

The speed control requirement of the motor drive system is about $10\mu s$ tolerance in time with respect to the actual zero-crossing. Because of the S/H nature of the sampled BEMF waveform, it will create jitter in speed control loop. This is overcome by slope compensation during hold time. In practice, only one direction slope compensation (either positive to negative or negative to position transition) is required. In the preferred embodiment, negative slope compensation is performed. The negative slope compensation technique is described below:

$$V_{bemf} = A * \sin (\omega * t),$$

Where

ω = angular speed of the motor in rad/sec

A = bemf amplitude

Thus, the slope of the bemf at zero-crossing is given by:

$$\frac{d}{dt} (V_{bemf}) = A * \omega$$

Now if a constant current is used to discharge the S/H capacitor to generate this slope for compensation then we can write:

$$\frac{I}{C_{sh}} = A * \omega$$

$$I = C_{sh} * A * \omega$$

This discharge can be achieved using a resistor having a value given by:

$$R_{sh} = \frac{V_{ref}}{I}$$

Figure 5 shows the typical compensated S/H output waveform.

To minimize the speed control loop jitter, the actual BEMF zero-crossing must occur only during the PWM on-time. Although PWM signal is synchronized with a spin clock signal (each positive edge of the clock will advance the phase one by one), there are occurrences when the PWM off-time may coincide with the BEMF zero-crossing causing the system to lose valuable zero-crossing information, particularly when the motor is speeding up. This is even more critical when the motor is transiting from start to run mode.

Using the reconstructed BEMF information a "window" is defined. During this "window" time, PWM chopping is inhibited and the corresponding drivers are turned on permanently. Upon successful zero-crossing detection, this window is disabled and normal PWM chopping resumes. During this window the PWM-on information is latched and provided to the controlling microprocessor to manipulate spin clock hence speed to ensure that zero-crossing must happen during PWM on time. After this operation, "window" mode will be permanently disabled.

The window time is set based on reconstructed BEMF as follows:

$$V_{bemf} = V_a * \sin (\pi - t_{win} * \omega)$$

For 7200rpm speed of motor and BEMF amplitude 4V:

$$\omega = \frac{7200}{60} * 4 * 2 \cdot \pi, (4\text{-pole pair motor})$$

Therefore, to set a window time, t_{win} of 25usec from a zero-crossing, the corresponding BEMF voltage is given by:

$$V_{bemf} = 0.251V$$

Figure 6 shows by changing the magnitude of the reference current which can be set externally through a resistor, the corresponding BEMF voltage is set as the reference voltage to which the reconstructed BEMF signal is compared. The advantage of this scheme is the capability to change the size of this window thereby allowing the detection scheme to operate even with BEMF signal as low as 100mV, thus facilitating the handover from start to run mode even at low motor speed.

A comparator compares the BEMF voltage with reference voltage (V_{ref}) and changes state upon BEMF voltage crosses the reference voltage each time. To avoid false transition near crossing, a small hysteresis (approximately 10mV) is introduced which changes its direction according to the slope.

The effect of the hysteresis is shown in Figure 7.

The foregoing describes only one embodiment of this invention and modifications can be made without departing from the scope of the invention.



CLAIMS

1. A method of detecting the back electromotive force in a three- phase brushless DC motor driven in half bridge configuration and operated continuously in a pulse width modulated mode, said method comprising the steps of obtaining a difference signal indicative of the difference between the centre tap voltage and the voltage of at least one of said phases during a tri-stated condition of that phase and producing from said difference signal a measure of said back electromotive force.
2. A method as claimed in claim 1, further comprising the step of obtaining said difference signal during an on cycle of said pulse width modulation.
3. A method as claimed in claim 2, further comprising the step of generating a reconstructed signal indicative of said back electromotive force from sequential difference signals by holding said reconstructed signal at a hold value determined by each said sequential difference signal until the next sequential difference signal is obtained.
4. A method as claimed in claim 3, wherein said reconstructed signal is adjusted between sequential difference signals by applying a slope compensation to each said hold value.
5. A method as claimed in claim 4, wherein said slope compensation is achieved by a linear adjustment of said hold value with time.
6. A method as claimed in claim 5, wherein said linear adjustment is determined by a calculation of the rate of change of said back electromotive force at the zero-crossing point for the motor operating speed.
7. A method as claimed in any one of claims 2 to 6, wherein said difference signal is obtained following a delay time from the commencement of said on cycle of said pulse

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indicative of the difference between the centre tap voltage and the voltage of at least one of said phases during a tri-stated condition of that phase and to produce from said difference signal a measure of said back electromotive force.

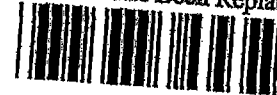
16. An apparatus as claimed in claim 15, wherein said difference signal is produced during an on cycle of said pulse width modulation.
17. An apparatus as claimed in claim 16, further comprising means to generate a reconstructed signal indicative of said back electromotive force from sequential difference signals by holding said reconstructed signal at a hold value determined by each said sequential difference signal until the next sequential difference signal is obtained.
18. An apparatus as claimed in claim 17, wherein said reconstructed signal is adjusted between sequential difference signals by applying a slope compensation to each said hold value.
19. An apparatus as claimed in claim 18, wherein said slope compensation is achieved by a linear adjustment of said hold value with time.
20. An apparatus as claimed in claim 19, wherein said linear adjustment is determined by a calculation of the rate of change of said back electromotive force at the zero-crossing point for the motor operating speed.
21. An apparatus as claimed in any one of claims 16 to 20, wherein said difference signal is obtained following a delay time from the commencement of said on cycle of said pulse width modulation.
22. An apparatus as claimed in claim 21, wherein said delay time is about 20% of the pulse width modulation on time.





23. An apparatus as claimed in any one of claims 15 to 22, further comprising a comparator to detect zero-crossing of said back electromotive force.
24. An apparatus as claimed in claim 23, wherein said pulse width modulation chopping is inhibited during a predetermined window prior to zero-crossing of said back electromotive force.
25. An apparatus as claimed in claim 24, wherein said inhibiting of pulse width modulating chopping ensures subsequent zero-crossing of said back electromotive force will occur during the on time of said pulse width modulation.
26. An apparatus as claimed in claim 24 or claim 25, wherein said window is determined from a reconstructed signal indicative of said back electromotive force by selecting a back electromotive force value below which said pulse width modulation chopping is inhibited.
27. An apparatus as claimed in any one of claims 15 to 26, wherein the back electromotive force is detected for each of said phases by multiplexing the voltages of each of said phases during the respective tri-stated condition of that phase to a single comparator.
28. An apparatus as claimed in claim 27, wherein said comparator is a differential amplifier with unit gain.

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