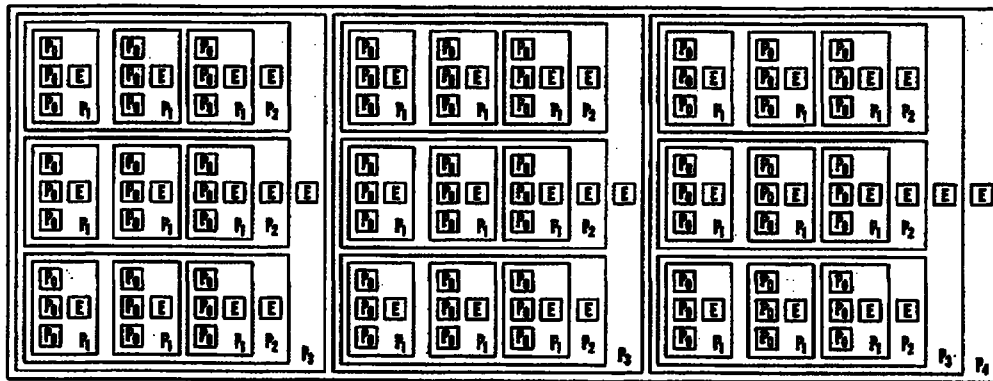




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : G06F 15/173, 15/76		A2	(11) International Publication Number: WO 00/22545
			(43) International Publication Date: 20 April 2000 (20.04.00)
(21) International Application Number: PCT/NO99/00308 (22) International Filing Date: 8 October 1999 (08.10.99) (30) Priority Data: 19984746 9 October 1998 (09.10.98) NO (71) Applicant (for all designated States except US): FAST SEARCH & TRANSFER ASA [NO/NO]; P.O. Box 1766 Vika, N-0120 Oslo (NO). (72) Inventors; and (75) Inventors/Applicants (for US only): HALAAS, Arne [NO/NO]; Overlege Bratts vei 60, N-7026 Trond- heim (NO). SVINGEN, Børge [NO/NO]; Borkdalen 6, N-7550 Hornmelvik (NO). LEISTAD, Geirr, I. [NO/NO]; Jongsstubbën 19, N-1337 Sandvika (NO). (74) Common Representative: LEISTAD, Geirr, I.; Opticom ASA, P.O. Box 1872 Vika, N-0124 Oslo (NO).		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>In English translation (filed in Norwegian).</i> <i>Without international search report and to be republished</i> <i>upon receipt of that report.</i>	

(54) Title: DIGITAL PROCESSING DEVICE



(57) Abstract

A digital processing device P, generally configured as a regular tree with $n+1$ levels $S_0, S_1, S_2, \dots, S_n$ and degree k , is provided in the form of a circuit P_n on the level S_n and forms the root node of the tree, an underlying level $S_{n-q}, q=1, 2, \dots, n-1$, in the circuit P comprising generally k^q circuits P_{n-q} provided nested in the k^{q-1} circuits P_{n-q+1} on the overlying level S_{n-q+1} , each circuit P_{n-q+1} on this level comprising k circuits P_{n-q} . A for $q=n$ defined zeroth level in the circuit P_n comprises from $k^{n-1}+1$ to k^n circuits P_0 which form kernel processors in the processing device P and on the level S_0 constitute the leaf nodes of the tree, the kernel processor P_0 being provided nested in a number from 1 to k in each of the circuits P_1 on the level S_1 . Each of the circuits $P_1, P_2, \dots, P_n$, comprises a logic unit E which generally is connected with circuits $P_0, P_1, \dots, P_{n-1}$ provided nested in the former circuits on the nearest underlying level and is additionally adapted to connect nodes on the same or underlying levels in neighbour trees. Each of the circuits $P_0, P_1, \dots, P_n$ has additionally identical interfaces I, such that $I_{P0}=I_{P1}=\dots=I_{Pn}$.