

ABSTRACT

APPARATUS FOR BINARY ADDITION

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An N-input m-bit high-speed adder tree circuit, where N and m are integers, employing Carry Select Addition and bit-sliced design configuration, is disclosed. The m bits of each input are split
10 into bit slice cells of predetermined length, which is determined according to total number of bits of input, so as to minimize the timing delay through the whole adder tree. Sum computation of each bit slice cell is performed independently and combined together to form the final result of the addition by implementing
15 Carry Select Addition.

Fig. 1