

SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

This invention relates to a semiconductor memory device and more particularly to a dynamic random access memory (hereinafter referred to as "dynamic RAM") having an operating mode in which data comprising a plurality of bits can be read out or written in serially.

The address multiplex system, in which address signals are applied twice separately as an address designation system, has been employed in a semiconductor memory device with a large memory capacity such as a 64K bit (65,536 bits) dynamic RAM, in order to reduce the number of pins on the package holding the memory device. When this address multiplex system is used for a 64K bit dynamic RAM, the number of pins on the package may be 16. In other words, the 64K bit dynamic RAM is placed in a 16-pin package.

The function of each pin is standardized, as shown in Figure 4, when packaging a 64K bit dynamic RAM in a 16-pin package. In other words, 16-bit address signals are applied in two separate halves to pins 5 -7 and pins 9 - 13. Pin 1 is generally used for

refresh, pins 2 and 14 are used as data input and output pins, and pin 3 as a write enable signal ($\overline{WE}$) input pin. Pins 4 and 15 are used as input pins for a row address strobe signal $\overline{RAS}$ (hereinafter referred to as " $\overline{RAS}$ signal") and a column address strobe signal $\overline{CAS}$ (hereinafter referred to as " $\overline{CAS}$ signal"), and pins 8 and 16 as power pins.

256K bit (= 262,144 bits) dynamic RAMs have been developed extensively in recent years. The number of address signals is greater in a 256K bit dynamic RAM than in a 64K bit dynamic RAM. In order to construct a 256K bit dynamic RAM while securing an input pin for refresh control signals, therefore, the design concept of the conventional 64K bit RAM must be changed to either increase the number of pins or detect the refresh timing from the relationship of the timings of the $\overline{RAS}$ and $\overline{CAS}$ signals, thereby making it possible to use pin 1 of the 16-pin package as an input pin for an address signal A_8 . However, compatibility between the 64K bit dynamic RAM and the 256K bit dynamic RAM is lost in the former case.

In order to develop a dynamic RAM having a greater memory capacity such as a 1M bit (= 1,024,000 bits) dynamic RAM, an increase in the number of pins is inevitable unless the design concept itself can be changed.

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According to a first aspect of the present invention there is provided a semiconductor memory device including:

- 5 (a) a memory cell array having a plurality of input-output terminals, ~~in which a plurality of input~~
~~output terminals~~ in which a plurality of memory cells are arranged so as to be selected substantially simultaneously and said memory cells thus selected are connected to said input-output terminals in a one-to-one
10 manner;
- (b) a first switch circuit connected to said input-output terminals of said memory cell array, and having a plurality of control terminals, the first switch circuit being arranged to selectively connect a said
15 input-output terminal to an input circuit in accordance with signals on the control terminals;
- (c) a second switch circuit connected to said input-output terminals of said memory cell array, and having a plurality of control terminals, the second switch
20 circuit being arranged to selectively connect a said input-output terminal to an output circuit in accordance with signals on the control terminals;
- (d) a control circuit outputting a control signal; and
- 25 (e) a selecting circuit arranged to receive the control signal output from said control circuit and a plurality of signals corresponding to a plurality of address signals, and to apply a plurality of selection signals to said control terminals of said first and
30 second switch circuits, for first selectively connecting one of said input-output terminals to said input circuit and said output circuit, and for thereafter selectively and sequentially connecting remaining input-output terminals other than said predetermined
35 one of said input-output terminals to said input circuit and said output circuit.

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According to a second aspect of the present invention there is provided a semiconductor memory device including:

- 5 (a) a memory cell array having a plurality of input-output terminals, in which a plurality of memory cells are arranged so as to be selected substantially simultaneously and said memory cells thus selected are connected to said input-output terminals in a one-to-one manner;
- 10 (b) a first switch circuit connected to said input-output terminals of said memory cell array and having a plurality of control terminals, the first switch circuit being arranged to selectively connect a said input-output terminal to an input circuit in accordance
15 with signals on the control terminals;
- (c) a second switch circuit connected to said input-output terminals of said memory cell array and having a plurality of control terminals, the second switch circuit being arranged to selectively connect a
20 said input-output terminal to an output circuit in accordance with signals on the control terminals;
- (d) a control circuit outputting a control signal; and
- (e) a selecting circuit arranged to output to
25 said control terminals of said first and second switch circuits a selection signal which connects a predetermined input-output terminal of said plurality of input-output terminals of said memory cell array to said input and output circuits, and thereafter to output to said control
30 terminals selection signals which connect sequentially and selectively a plurality of input-output terminals other than said predetermined input-output terminal to said input and output circuits in response to the control signal output from said control circuit.

35 According to a third aspect of the present invention there is provided a semiconductor memory device including:

(a) a memory cell array having a plurality of input-output terminals, in which a plurality of memory cells are arranged so as to be selected substantially simultaneously and said memory cells thus selected are
5 connected to said input-output terminals in a one-to-one manner;

(b) a switch circuit connected to said input-output terminals of said memory cell array, and having a plurality of control terminals, the switch circuit being
10 arranged to selectively connect a said input-output terminal to an input circuit in accordance with signals one the control terminals;

(c) a control circuit outputting a control signal; and

15 (d) a selecting circuit arranged to receive the control signal output from said control circuit and a plurality of signals corresponding to a plurality of address signals, and to apply a plurality of selection signals to said control terminals of said switch circuit,
20 for first selectively connecting a predetermined one of said input-output terminals to said input circuit and for thereafter selectively and sequentially connecting remaining input-output terminals other than said predetermined one of said input-output terminals to said
25 input circuit.

According to a fourth aspect of the present invention there is provided a semiconductor memory device including:

(a) a memory cell array having a plurality of
30 input-output terminals, in which a plurality of memory cells are arranged so as to be selected substantially simultaneously and said memory cells thus selected are connected to said input-output terminals in a one-to-one manner;

35 (b) a switch circuit connected to said input-output terminals of said memory cell array, and having a plurality of control terminals, the switch

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circuit being arranged to selectively connect a said input-output terminal to an output circuit in accordance with signals on the control terminals;

5 (c) a control circuit outputting a control signal; and

(d) a selecting circuit arranged to receive the control signal output from said control circuit and a plurality of signals corresponding to a plurality of address signals, and to apply a plurality of selection
10 signals to said control terminals of said switch circuit, for first selectively connecting a predetermined one of said input-output terminals to said output circuit and for thereafter selectively and sequentially
connecting remaining input output terminals other than
15 said predetermined one of said input-output terminals to said output circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a semiconductor memory device in accordance with one embodiment of the
20 present invention;

Figure 2 is a timing chart of the device of Figure 1 when operating normally;

Figure 3 is a timing chart of the device when in nibble mode;

25 Figure 4 is a schematic view of the arrangement of the pins of a 16-pin package when it contains a

semiconductor memory device having a memory capacity of 64K bits or more;

Figure 5 is a circuit diagram of the device in accordance with one embodiment of the present invention; and

Figure 6 is a block diagram of an example of the selecting circuit 7 shown in Figure 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 is a block diagram of a 256K bit dynamic RAM to which the present invention is applied. The so-called "nibble mode" function which can read and write serial data comprising a plurality of bits, such as 4 bits, is added to the dynamic RAM of this embodiment. The dynamic RAM of this embodiment can be also used as an ordinary 256K bit dynamic RAM by utilizing the first pin as an input pin for an address signal A_8 .

In the diagram, all the circuit blocks encircled by the broken line are formed on a single semiconductor substrate by known semiconductor integrated circuit techniques. Terminals D_{in} , WE, $\overline{RAS}$, $\overline{CAS}$, D_{out} , V_{cc} , V_{ss} and A_0 through A_8 are connected to the corresponding pins provided on the package. When this 256K bit dynamic RAM is used only in the nibble mode, however, the address of the most significant bit, the address signal A_8 in this embodiment, is not provided

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as will be described later. Hence terminal A_8 may be omitted and a refresh control terminal, for example, could be provided instead of this address signal terminal A_8 , connected to the corresponding pin (pin 1) of the package. It will be necessary in such a case to provide the circuit necessary for the refresh operation on the 256K bit dynamic RAM, and apply a control signal controlling the operation to the refresh control terminal.

In the block diagram, reference numeral 1 represents a memory cell array, which is divided into four memory cell matrices 1a, 1b, 1c and 1d. Each memory cell matrix 1a - 1d has a 64K bit memory capacity. In other words, 65,536 memory cells in each memory matrix are arranged in a matrix of 512 (rows) by 128 (columns). The memory cell matrices are disposed symmetrically about X decoders 2a, 2b and Y decoders 3a, 3b at the center.

Reference numeral 4 represents an address buffer circuit. A plurality of address signals are divided in two and each half applied successively from a micro-processor (hereinafter referred to as "CPU"), not shown, to the address buffer circuit 4. X address signals $A_{x0} - A_{x8}$ and Y address signals $A_{y0} - A_{y8}$ are applied in a time-sharing manner from the CPU to the address buffer circuit 4.

The address buffer circuit 4 consists of a number of unit address buffers corresponding to the number of bits of the address signals applied to the buffer circuit 4. In this embodiment it consists of 18 unit address buffers. The unit address buffers have the same construction and each has a latch function holding the input address signals, although this is not particularly essential.

Reference numerals 5a and 5b represent internal control signal generators. The internal control signal generator 5a generates suitable control signals $RAS2$, ϕ_x and ϕ_{PA} on the basis of $\overline{RAS}$ signals applied thereto from the CPU. The internal control signal generator 5b generates suitable control signals $CAS1$, $CAS2$, $\overline{CAS3}$, ϕ_y , ϕ_{ma} and ϕ_{OP} on the basis of the $\overline{CAS}$ signals applied thereto from the CPU.

The signal $RAS2$ output from the internal control signal generator 5a is applied to the address buffer circuit 4. When the external $\overline{RAS}$ signal falls from high level to low level, the signal $RAS2$ rises in synchronism with it, as shown in Figure 2. Accordingly, the address buffer circuit 4 takes in and latches the X address signals $A_{x0} - A_{x8}$ and outputs both internal address signals $a_{x0} - a_{x8}$ corresponding to the address signals $A_{x0} - A_{x8}$, and internal address

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signals $\overline{a}_{x0} - \overline{a}_{x8}$ that are phase-inverted with respect to the address signals $A_{x0} - A_{x8}$.

The signal ϕ_x (word line selection timing signal) output from the internal signal generator 5a and the internal address signals a_{xi} , $\overline{a}_{xi}$ ($i = 0 - 7$) output from the address buffer circuit 4 are applied to the X decoders 2a and 2b, respectively. The word line selection timing signal ϕ_x rises to high level shortly after the signal RAS2 when the $\overline{RAS}$ signal falls to low level. Accordingly, the right and left X decoders 2a and 2b each select one word line determined by the internal address signals a_{xi} , $\overline{a}_{xi}$ ($i = 0 - 7$) supplied from the address buffer circuit 4, and bring the lines to a selection level. In other words, a word line determined by the address signals $A_{x0} - A_{x7}$ is selected from each of the memory cell matrices 1a - 1d. When the signal ϕ_{PA} applied from the internal signal generator 5a to each memory cell matrix 1a - 1d rises next, the data from all the memory cells connected to the word lines selected by the X decoders 2a, 2b are amplified by corresponding pre-amplifiers (not shown), and are each latched.

The signal CAS2 output from the internal signal generator 5b is also applied to the address buffer circuit 4 in the same way as the signal RAS2. When

the external $\overline{\text{CAS}}$ signal falls from high level to low shortly after the $\overline{\text{RAS}}$ signal described above, the signal CAS2 rises in synchronism with it, as shown in Figure 2. When this happens, the address buffer circuit 4 takes in the Y address signals $A_{y0} - A_{y8}$ applied thereto and latches them. The buffer 4 then outputs both internal address signals $a_{y0} - a_{y8}$ corresponding to the address signals $A_{y0} - A_{y8}$, and internal address signals $\overline{a}_{y0} - \overline{a}_{y8}$ that are phase-inverted with respect to the address signals $A_{y0} - A_{y8}$. Of these internal address signals, the internal address signals $a_{y0} - a_{y7}$ and $\overline{a}_{y0} - \overline{a}_{y7}$ are applied to the Y decoders 3a, 3b, respectively.

The signal ϕ_y (data line selection timing signal) generated by the internal signal generator 5b is applied to the Y decoders 3a and 3b. The data line selection timing signal ϕ_y rises a little after the signal CAS2 , as shown in Figure 2. When the signal ϕ_y rises, the Y decoders 3a and 3b each select one data line (or a data line pair) corresponding to the address signals $A_{y0} - A_{y7}$ from the memory matrices 1a - 1d.

The signal ϕ_{ma} generated by the internal signal generator 5b is applied to four main amplifiers MA1 through MA4. The signal ϕ_{ma} rises a little after the data line selection timing signal ϕ_y , as shown in

Figure 2. When the signal ϕ_{ma} rises, the data that is latched by four pre-amplifiers connected to the four data lines (or four data line pairs) selected by the Y decoders 3a and 3b are simultaneously amplified by the main amplifiers MA1 - MA4 and are latched.

The $\overline{RAS}$ signal and the $\overline{CAS}$ signal are also applied to a changing signal generator 6. When pin 1 of the package containing the semiconductor memory device is used as an input pin for an address signal, namely when the address signals A_{x8} and A_{y8} (the bits with the highest addresses) are applied to pin 1 in a time-sharing manner, the $\overline{RAS}$ signal goes from high level to low, and then the $\overline{CAS}$ signal goes from high level to low. Thereafter these signals are kept at low level. Accordingly, the changing signal generator 6 produce a control signal ϕ_{NF} of low level. In response to the control signal ϕ_{NF} of low level, a gate Ga is opened, and a gate circuit Gb outputs a control signal CAS1 as a control signal ϕ_C .

Reference numeral 7 represents a selecting circuit. Figure 6 is a block diagram of an example of this selecting circuit 7. The selecting circuit 7 consists of a latch circuit 12 which latches the internal address signals a_{x8} , $\overline{a_{x8}}$ and a_{y8} , $\overline{a_{y8}}$ applied thereto in a time-sharing manner, a decoder 13 for decoding signals output from the latch circuit 12, that is,



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the internal address signals, and a shift register 11 for receiving decoded signals output from the decoder 13. The shift register 11 consists of four registers 11-1, 11-2, 11-3 and 11-4 that correspond in a one-to-one way to the decoded signals from the decoder 13. When the control signal (shift pulse) ϕ_c rises to high level, for example, each register receives either the corresponding decoded signal from the decoder 13 or the signal output from the register of the preceding stage as its input signal, and outputs a signal corresponding to the input signal when the shift pulse ϕ_c falls to low level. Each register consists of a one-bit memory circuit such as a flip-flop circuit, although this is not particularly essential.

In the normal mode, the gate Ga is opened by the control signal ϕ_{NF} of low level from the changing signal generator 6, and the internal address signals a_{x8} , $\overline{a_{x8}}$, a_{y8} and $\overline{a_{y8}}$ are applied to the latch circuit 12 in a time-sharing manner through this gate Ga. The internal address signals thus latched in the latch circuit 12 are input to, and decoded by, the decoder 13. Each decoded signal is applied to the corresponding register. At the same time, the control signal CAS1 is applied to each register as the control signal ϕ_c . The control signal CAS1 is a pulse signal with a pre-

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determined pulse width that is formed in synchronism with the $\overline{\text{CAS}}$ signal falling to low level. When this pulse signal rises to high level, for example, each register takes in the decoded signal supplied from the decoder 13, and produces a decoded signal as its output when the pulse signal falls to low level. Accordingly, one of output lines $N_1 - N_4$ connected to these registers is brought to high level, and the others to low level. One of gates $G_1 - G_4$ is opened by the output line of the selecting circuit 7 which is high level, so that one unit of the data latched in the main amplifiers MA1 - MA4 is applied to an output buffer circuit 8 and is output externally.

In other words, in the data read from each of the 4 memory cell matrices, only the data determined by the address signals A_{x8}, A_{y8} (highest address bits) is applied to the output buffer circuit 8. The output buffer circuit 8 outputs the applied data at the timing of the signal ϕ_{Op} output from the internal signal generation circuit 5b.

Reference numeral 9 represents an input buffer circuit to which data is applied externally. Reference numeral 10 represents a read/write control signal generator to which a write enable signal $\overline{\text{WE}}$ is applied. The write enable signal $\overline{\text{WE}}$ is kept at high level during the data reading operation. In



response to this high-level write enable signal $\overline{WE}$, the read/write control signal generator 10 produces a signal RW2 of a potential that renders the input buffer circuit 9 inoperative. Accordingly, the input buffer circuit 9 is kept inoperative during the data reading operation.

The write enable signal $\overline{WE}$ is kept at low level during the data writing operation. In response to the low-level write enable signal $\overline{WE}$, the read/write control generator 10 produces a signal RW2 of a potential that renders the input buffer circuit 9 operative. Hence the input buffer circuit 9 is made operative, and generates an output signal which corresponds to the data D_{in} applied thereto externally. The selecting circuit 7 operates in the same way as during the reading operation described above. Thus the selecting circuit 7 opens only one of four gates g_1 through g_4 that is determined by the input address signals A_{x8} and A_{y8} . The signal output from the input buffer circuit 9 is sent to the corresponding driver of four drivers $d_{in1} - d_{in4}$ through the gate that has been opened.

A signal output from the driver which has received the signal output from the input buffer circuit 9 is applied to the memory array 1 via the

corresponding main amplifier of the four main amplifiers MA1 - MA4. The X decoders 2a, 2b and the Y decoders 3a, 3b each select one memory cell from the memory cell matrices 1a - 1d determined by the address signals $A_{x0} - A_{x7}$ and $A_{y0} - A_{y7}$ applied to these decoders. The memory cell matrices and the main amplifiers correspond in a one-to-one way. A signal output from the main amplifier of the four main amplifiers MA1 - MA4 which has received the signal output from the input buffer circuit 9 is applied to, and written into, the selected memory cell of the corresponding memory cell matrix.

In this case (during the data writing operation), the signal ϕ_{Op} of a potential (high level) that renders the output buffer circuit 8 operative is not applied to the buffer circuit 8 from the internal signal generator 5b, so that the buffer circuit 8 does not operate. The signal ϕ_{Op} is generated on the basis of the control signal RW2 from the read/write control signal generator 10, or the like, and goes low level when data is to be written in. The signal ϕ_{Op} goes high level when data is to be read out.

When the 256K bit dynamic RAM is used in the nibble mode, the address signals $A_{x0} - A_{x8}$ and $A_{y0} - A_{y8}$ are taken into the address buffer circuit 4 as a



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result of the first fall of the $\overline{\text{RAS}}$ signal and the first fall of the $\overline{\text{CAS}}$ signal, in the same way as in the normal operating mode described above. Accordingly, one memory cell is selected from each of the four memory cell matrices by the address signals $A_{x0} - A_{x7}$ and $A_{y0} - A_{y7}$ in the same way as in the normal operating mode described above, and one memory cell is selected by the address signals A_{x8} and A_{y8} from the four memory cells thus selected. In other words, the selecting circuit 7 changes only one output line determined by the address signals A_{x8} and A_{y8} to high level, and the rest to low level.

In the nibble mode, the $\overline{\text{CAS}}$ signal is made to change with a short period, as shown in Figure 3, while the $\overline{\text{RAS}}$ signal is kept at low level.

The changing signal generator 6 judges whether the mode is normal mode or nibble mode from the $\overline{\text{RAS}}$ signal and the $\overline{\text{CAS}}$ signal. When the $\overline{\text{CAS}}$ signal falls to low level after the $\overline{\text{RAS}}$ signal has fallen to low level and the $\overline{\text{CAS}}$ signal does not change thereafter (normal mode), the changing signal generator 6 produces the low-level control signal ϕ_{NF} as described above. When the $\overline{\text{CAS}}$ signal falls to low level after the $\overline{\text{RAS}}$ signal has fallen to low level and the $\overline{\text{CAS}}$ signal changes again thereafter (nibble mode), the control signal ϕ_{NF} is changed from low level to

high level in synchronism with the second fall of the $\overline{\text{CAS}}$ signal to low level. Since the control signal ϕ_{NF} is thus changed to high level, the gate Ga is closed and the gate Gb produces a control signal CAS' as the control signal ϕ_c .

Since the gate Ga is closed, the signals (the internal address signals a_{x8} , $\overline{a}_{x8}$, a_{y8} , $\overline{a}_{y8}$) output from the address buffer circuit 4 are no longer applied to the selecting circuit 7. The gate Gb applies the control signal CAS' as the control signal ϕ_c to the selecting circuit 7, so that it operates like a shift register. The control signal CAS' is a signal that is formed based on the $\overline{\text{CAS}}$ signal and rises to high level in synchronism with the fall of the $\overline{\text{CAS}}$ signal to low level. When the $\overline{\text{CAS}}$ signal again falls, the control signal CAS' rises again in response, as shown in Figure 3. In other words, in the nibble mode the control signal CAS' becomes a pulse signal which repeatedly rises from low level to high then falls from high level to low.

The output line of the selecting circuit 7 which first becomes high level in nibble mode is determined by the address signals A_{x8} and A_{y8} that are taken in at the fall of the $\overline{\text{RAS}}$ signal and at the fall of the $\overline{\text{CAS}}$ signal, in the same way as in the normal mode.

In other words, the selecting circuit 7 operates in the nibble mode in the same way as in the normal mode until the $\overline{\text{RAS}}$ signal changes, and the $\overline{\text{CAS}}$ signal changes and changes once again. Assume, for example, that the decoder 13 outputs to the register 11-2 a decoded signal of high level by the internal address signals a_{x8} , $\overline{a_{x8}}$, a_{y8} and $\overline{a_{y8}}$ that are shaped based on the address signals A_{x8} and A_{y8} taken in at the fall of the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals, and decoded low-level signals to the rest of the registers. In this case, since the shift clock ϕ_c (control signal CAS1) changes to high level, each register takes in the corresponding decoded signal from the decoder 13. When the shift clock ϕ_c (control signal CAS1) falls to low level, the signal output from the register 11-2 changes to high level and the outputs of the rest change to low level. The $\overline{\text{CAS}}$ signal then rises to high level. In synchronism with the rise of this $\overline{\text{CAS}}$ signal to high level, the internal control signal generator 5b produces the high-level control signal $\overline{\text{CAS3}}$. When the control signal $\overline{\text{CAS3}}$ rises to high level, the decoder 13 inside the selecting circuit 7 is rendered inoperative, and at the same time the signals output from the decoder 13 are not actually applied to the registers. Accordingly each register takes in the signal output from its preceding

stage as its input.

In other words, when the $\overline{\text{CAS}}$ signal again falls to low level, the control signal ϕ_{NF} becomes high level and the control signal CAS' is applied as the shift clock ϕ_c to each register. When this shift clock ϕ_c (control signal CAS') rises to high level, the register 11-1, for example, receives the signal output from the register 11-2 of the preceding stage as its input and, similarly, the register 11-2 receives the signal output from the register 11-3 as its input. Since the shift register 11 consists of a loop of these registers 11-1 through 11-4, the register 11-4 receives the output from the register 11-1 of the preceding stage as its input.

Next, when the CAS' signal again falls to low level, each register outputs a signal corresponding to the input signal taken into that register. In the embodiment described above, therefore, the signal output from the register 11-1 becomes high level when the CAS' signal falls, and the signals output from the rest of the registers 11-2 through 11-4 change to low level. Whenever the $\overline{\text{CAS}}$ signal again rises to high level and falls to low level, the operation described above is repeated. In other words, the registers 11-2, 11-1, 11-4 and 11-3 output high-level signals in order.

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That is, whenever the $\overline{\text{CAS}}$ signal changes, the output lines N_2 , N_1 , N_4 and N_3 become high level in turn.

Accordingly, the gate circuits G_1 through G_4 ($g_1 - g_4$) corresponding to the respective output lines of the selecting circuit 7 open sequentially. In the embodiment described above, the gate circuit G_2 (g_2) opens first and every time the $\overline{\text{CAS}}$ signal falls, the gate circuits G_1 , G_4 and G_3 (g_1 , g_4 , g_3) open sequentially. Thus, the gates G_1 to G_4 and the gates g_1 to g_4 respectively form output and input switch circuits. These gates can be formed from insulated gate field effect transistors.

As described previously, one memory cell is selected from each of the four memory matrices by the address signals $A_{x0} - A_{x7}$ and $A_{y0} - A_{y7}$. Hence, the main amplifiers MA_1 through MA_4 corresponding to these memory matrices amplify and latch the data from the memory cells selected from the corresponding memory cell matrices.

Accordingly, one gate circuit is first opened by the address signals A_{x8} and A_{y8} and the data latched in the corresponding main amplifier is applied to the output buffer circuit 8 and output from it. Next, every time the $\overline{\text{CAS}}$ signal falls, the data latched in the remaining main amplifiers are applied sequentially to the output buffer circuit 8 and are read out sequentially. In the example described above, the data latched in the main amplifier MA_2 is output first,

followed by the data latched in the main amplifier MA_1 , that in MA_4 , and that in MA_3 .

Since the shift register 11, which operates so as to read out the 4-bit data from the main amplifier in the nibble mode, is driven by changes in the $\overline{CAS}$ signal in the manner described above, the data can be read out at a higher speed than in the conventional system in which the data is read out bit-by-bit from the memory cell array by changing the address signals.

When the data is written in the nibble mode, the read/write control signal generator 10 generates a control signal RW2 that renders the input buffer circuit operative, in accordance with the write enable signal $\overline{WE}$ of low level. In this case, the output buffer circuit 8 is rendered inoperative by the signal ϕ_{Op} . In a write operation, as with the read operation described above, the shift register 11 in the selecting circuit 7 is operated by the change in the $\overline{CAS}$ signal. Thereby the 4-bit data is written sequentially into the memory cells of the corresponding memory matrix of the memory matrices 1a - 1d through the gate circuits $g_1 - g_4$.

Assume, for example, that in the same way as in the read operation described above, the output line N_2 of the selecting circuit 7 is first to become high level and the output lines N_1 , N_4 , and N_3 in order become high level sequentially in accordance with the

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change of the $\overline{\text{CAS}}$ signal. The first unit of data is transmitted to a memory cell inside the memory matrix 1b, for example, via the gate g_2 , and the next item of data is transmitted to a memory cell in the memory cell matrix 1a via the gate g_1 . Similarly, the subsequent data is transmitted and written into a memory cell in the memory matrix 1d via the gate g_4 , and into a memory cell inside the memory matrix 1c via the gate g_3 , respectively. In the memory matrices 1a - 1d, the memory cells into which the data is written are the memory cells determined by the address signals A_{x0} - A_{x7} and A_{y0} - A_{y7} . To prevent unwanted data from being written into the memory cells, the control signal ϕ_c is applied to the input buffer circuit 9. This circuit 9 takes in external data in synchronism with the control signal ϕ_c to prevent unwanted data from being transmitted to the memory cells.

When the $\overline{\text{RAS}}$ signal and the $\overline{\text{CAS}}$ signal fall to low level to read out or write in data after this dynamic RAM has been used in the nibble mode, new internal address signals corresponding to the address signals that will be used this time are applied to the latch circuit 12 via the gate Ga. The internal control signal generator 5b outputs the control signal $\overline{\text{CAS3}}$ of low level. This means that the decoder 13

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receives new internal address signals, decodes them and applies the decoded signals to the shift register 11. When the shift clock ϕ_c rises to high level, the shift register 11 takes in the decoded signals; and when the shift clock ϕ_c falls to low level, the shift register 11 outputs signals corresponding to the decoded signals that were taken into it. If the subsequent operating mode is normal mode, the normal mode operation described above is executed; and if it is nibble mode, the nibble mode operation is executed as described above.

In the nibble mode, 4-bit data can be read out or written in serially in the manner described above simply by changing the $\overline{\text{CAS}}$ signal once the X address signals $A_{x0} - A_{x8}$ and the Y address signals $A_{y0} - A_{y8}$ are applied. In the normal operating mode, data can be read out or written into one desired memory cell by using pin 1 as the address signal pin A_8 and applying the address signals A_{x8} and A_{y8} in a time-sharing manner. In other words, the RAM of this embodiment can be used as an ordinary 256K bit RAM even in the nibble mode.

When the semiconductor memory device of this embodiment is used in nibble mode, the address signals applied to the same pin in the time sharing are used

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as address signals that determine the initial state of the shift resistor used for selecting one memory cell from a plurality of memory cells selected from the memory cell array. Accordingly, if signals which correspond to the address signals are generated inside the semiconductor memory device, this pin can be used for purposes other than as the input pin for the address signals.

For example the following construction may be employed. First an input node N_{11} of the address signal A_8 of the address buffer circuit 4 is isolated electrically from the address signal input pin (pin 1) shown in Figure 4 and the node N_{11} is then connected to a predetermined potential point such as the ground potential point of the circuit. Then, as shown in Figure 5, an input node N_5 of invertors IV_1, IV_2 forming the address signals a_{x8} and $\overline{a_{x8}}$ from the X address signal A_{x8} and an input node N_6 of invertors IV_3, IV_4 forming the address signals a_{y8} and $\overline{a_{y8}}$ from the Y address signal A_{y8} are each set to predetermined potentials. Nodes N_7 through N_{10} shown in the figure are each connected to predetermined potentials. According to this arrangement, the address signal input pin (pin 1) can be used for other purposes. In such a case, the address buffer circuit 4 comprises the circuit as shown in Figure 5 and a multiplexor provided between the node N_{11} and nodes N_5 and N_6 . The multiplexor is controlled by control signals (not shown in Figures 1 and 3)

applied from the generators 5a and 5b. Since the multiplexor operates in a time sharing manner, address signals A_{x8} and A_{y8} are applied to nodes N_5 and N_6 through the multiplexor respectively. If pin 1 thus saved is used as a pin for a refresh control signal, the dynamic RAM of this embodiment can be made compatible with conventional 64K bit RAMs; and its capacity can be increased. In such a case, the circuit necessary for the refresh operation must be provided within this semiconductor memory device.

If the address signals that would be applied externally to the same pin in a time-sharing way are generated within the semiconductor memory device as described above, the memory device always operates in nibble mode. Since the address signals A_{x8} and A_{y8} are always kept at respective predetermined potentials, the address signals A_{x8} and A_{y8} that are taken in at the first fall of the $\overline{RAS}$ signal and at the first fall of the $\overline{CAS}$ signal are always constant signals. Accordingly, that register of the plurality of registers forming the shift register 11 which first generates a high-level output signal is always the same in nibble mode. For this reason, the sequence of memory matrices from which the data is read, or into which it is written, is always the same.

If the signals applied to the selecting circuit 7 are generated within the semiconductor memory device as described above, the gate G_a can be omitted provided that measures are taken to prevent the signals output from the selecting circuit 7 from exerting any adverse influence on the address buffer circuit 4.

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If the nodes N_7 through N_{10} in Figure 4 are connected to their respective predetermined potentials in order to generate the signals to be applied to the selecting circuit 7 within the semiconductor memory device, the invertors IV_1 through IV_4 for the address signal A_8 can be omitted. This results in a reduction of the chip area and the production cost. However, the nodes N_7 and N_8 and the nodes N_9 and N_{10} must be connected to mutually different potentials (e.g., V_{ss} and V_{cc}).

In Figure 6, a circuit which outputs signals having predetermined voltages to the shift register 11 when the shift pulse ϕ_c (control signal CAS1) goes high level may be provided in place of the decoder 13 and the latch circuit 12. For example, a circuit may be provided which outputs a high-level signal to the register 11-1 and low-level signals to the rest of the registers.

Although the above description deals with the case in which signals corresponding to the address signals to be applied externally to the same pin in a time-sharing manner are generated within the semiconductor memory device itself, a predetermined potential may be applied to pin 1 instead. For example, the ground potential of the circuit may be applied steadily to pin 1. In this case, the semiconductor memory device

operates in nibble mode in the same way as when the address signals are generated within the semiconductor memory device. In this case, further, the number of address signals for the 256K bit dynamic RAM is equal to the number of address signals for a 64K bit dynamic RAM in the same way as when signals corresponding to the address signals are generated within the semiconductor memory device and, moreover, since the pin arrangement of the package of the 256K bit dynamic RAM is substantially the same as that of a 64K bit dynamic RAM, compatibility can be established between a conventional 64K bit dynamic RAM and the 256K bit dynamic RAM, and the capacity of the memory in the 16-pin package can be increased.

The refresh control signal may be applied to pin 1 in the same way as in a conventional 64K bit dynamic RAM. In this case, the refresh operation and the nibble operation are executed in a time sharing manner, that is, the data read or write operation may be executed when the refresh control signal is at a predetermined potential (e.g. high potential) and the refresh operation may be executed when the refresh control signal is at another potential (e.g. low potential). In this manner, a memory having a large capacity can be obtained easily.

In the semiconductor memory device of the embodiment described above, the address signals applied to the same pin in a time-sharing manner are used as address signals which determine the initial stage of the shift

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register used for selecting one memory cell from the plurality of memory cells selected from the memory cell array. For this reason this semiconductor memory device can be operated easily in nibble mode simply by making this pin be at the predetermined potential. However, the semiconductor memory device cannot be operated in nibble mode unless the voltages (signals) applied to different pins change with time if the initial stage of the shift register is determined by address signals applied to different pins. In other words, a specific circuit is needed to change the voltages (signals) applied to the pins on a time basis.

The pin arrangement of the package containing the dynamic RAM of this embodiment is the same as that of a conventional 64K bit dynamic RAM with the only exception being pin 1. Accordingly, a 64K bit dynamic RAM can be upgraded to a 256K bit dynamic RAM simply by changing the wiring.

In the embodiment described above, single bits of data which are stored in the memory cells selected by the address signals $A_0 - A_7$ are simultaneously read and latched by each of four main amplifiers, and a shift register is actuated by a $\overline{CAS}$ signal so as to sequentially output the data latched in the main amplifiers. Thus data can be read in at high

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speed. In normal mode, a selecting circuit 7 including the shift register is actuated by the most significant bit provided at pin 1 so as to select one memory cell from the four memory cells selected from the four memory cell matrices. This results in a structural advantage for the circuit because a 1M bit (= 1,048,576 bits) dynamic RAM can be obtained easily on the basis of the same design concept as the 256K bit dynamic RAM in the following manner without changing the design of the address decoder too much. First, a memory cell array of 1M bit is divided into four memory cell matrices (each having a memory capacity of 256K bits) of the same construction, and one memory cell is selected from each of the memory matrices by address signals $A_0 - A_8$. The selecting circuit 7 which always operates in nibble mode further selects one memory cell from the four memory cells thus selected. If pin 1 is used as the input pin for the address signal A_8 , the 1M bit semiconductor memory device can be packaged in a 16-pin package.

The present invention is not particularly limited to the embodiment described above. For example, the number of memory cell matrices forming the memory cell array may be increased, and the output data from the memory matrices may be output serially by the shift register or a similar devices.

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In such a case, the capacity of the memory device can be increased without increasing the number of pins for the address signals by sequentially allotting input data supplied externally to the memory cell matrices by the shift register or the like in the write operation as well. Thus even a semiconductor memory device having a memory capacity of 1M bit or more can be mounted in a 16-pin package. Each of the registers described may be of the type that receives a signal output from the decoder 13 as its input when the control signal ϕ_{NF} is low level, and receives a signal output from the register of a preceding stage as its input signal when the control signal ϕ_{NF} is high level.



CLAIMS.

1. A semiconductor memory device including:

(a) a memory cell array having a plurality of input-output terminals, in which a plurality of memory cells are arranged so as to be selected substantially simultaneously and said memory cells thus selected are
5 connected to said input-output terminals in a one-to-one manner;

(b) a first switch circuit connected to said input-output terminals of said memory cell array, and
10 having a plurality of control terminals, the first switch circuit being arranged to selectively connect a said input-output terminal to an input circuit in accordance with signals on the control terminals;

(c) a second switch circuit connected to said
15 input-output terminals of said memory cell array, and having a plurality of control terminals, the second switch circuit being arranged to selectively connect a said input-output terminal to an output circuit in accordance with signals on the control terminals;

(d) a control circuit outputting a control
20 signal; and

(e) a selecting circuit arranged to receive the control signal output from said control circuit and a plurality of signals corresponding to a plurality
25 of address signals, and to apply a plurality of selection signals to said control terminals of said first and second switch circuits, for first selectively





connecting one of said input-output terminals to said input circuit and said output circuit, and for thereafter selectively and sequentially connecting remaining input-output terminals other than said predetermined one of said input-output terminals to said input circuit and said output circuit.

2. A semiconductor memory device according to claim 1, further including:

(f) a second selecting circuit having a plurality of output terminals, and second selecting circuit receiving the plurality of signals corresponding to said address signals, and outputting a plurality of second selection signals determined by said plurality of signals thus received; and

(g) a shift register consisting of a plurality of registers corresponding in a one-to-one manner to said output terminals of said second selecting circuit, said shift register receiving said second selection signals applied via said output terminals corresponding thereto and said control signals output from said control circuit, and outputting selection signals which cause the first and second switch circuits to connect one of the input-output terminals of said memory cell array determined by said second selection signals to said input and output circuits, and then outputting further such selection signals which cause the first and second circuits to selectively and sequentially connect the



other said input-output terminals of said memory cell array to said input and output circuits, every time said shift register is operated on by the control signal.

3. A semiconductor memory device according to
5 claim 2, wherein said second selecting circuit comprises a decoder circuit decoding the plurality of signals corresponding to the plurality of said address signals.

4. A semiconductor memory device according to
10 claim 3, wherein the plurality of said signals corresponding to said plurality of address signals which are applied to said second selecting circuit consist of first signals based on first address signals applied at a first point in time and second signals based on second address signals applied at a second point in time.

15 5. A semiconductor memory device according to claim 4, wherein said control circuit comprises a first terminal to which a first control signal determining said first point in time is applied, a second terminal to which a second control signal determining said second
20 point in time is applied, and a second control circuit outputting said control signal for operating said shift register when said first and second control signals are applied to said first and second terminals at a predetermined timing relationship, so that memory cells are
25 selected sequentially from said plurality of memory cells selected from said memory cell array and are connected to said input and output circuits.





6. A semiconductor memory device according to claim 5, further including a third selecting circuit outputting selection signals for selecting said plurality of memory cells from said memory cell array, and in which said memory cells thus selected are connected to said input-output terminals of said memory cell array, thereby executing the writing or reading of data into or from said selected memory cells via said input-output terminals.
- 10 7. A semiconductor memory device according to claim 6, wherein said third selecting circuit comprises a first buffer circuit which receives a first address signal supplied at the first point in time and a second address signal applied at the second point in time and
15 applies said first and second signals to said decoder circuit; a second buffer circuit which receives a plurality of third address signals applied at said first point in time, and a plurality of fourth address signals supplied at said second point in time, and
20 outputs a plurality of third signals based on said plurality of third address signals and a plurality of fourth signals based on said plurality of fourth address signals; and a second decoder circuit which receives the plurality of said third and fourth signals
25 and outputs selection signals for selecting said plurality of memory cells from said memory cell array.



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8. A semiconductor memory device according to claim 7, wherein said third selecting circuit further includes a common terminal receiving said first address signal supplied at the first point in time and said
5 second address signal supplied at the second point in time, and in which said first and second address signals are applied from said common terminal to said first buffer circuit.

9. A semiconductor memory device according to
10 claim 8, wherein said device is packaged in a package having a plurality of pins and in which said common terminal of said third selecting circuit is connected to one of said plurality of pins.

10. A semiconductor memory device according to
15 claim 9, wherein said pin to which said common terminal of said third selecting circuit is connected is pin 1.

11. A semiconductor memory device according to any one of the preceding claims, wherein said memory cell array consists of a plurality of memory cell
20 matrices each containing a plurality of memory cells, and each of said memory cell matrices has one of said plurality of input-output terminals.

12. A semiconductor memory device according to any one of the preceding claims, wherein said first and
25 second switch circuits consist of a plurality of gate circuits.



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13. A semiconductor memory device according to any one of claims 4 to 10, wherein said selecting circuit comprises a latch circuit arranged to latch said first signals and said second signals and to apply said latched
5 first and second signals to said decoder circuit.

14. A semiconductor memory device including:

(a) a memory cell array having a plurality of input-output terminals, in which a plurality of memory cells are arranged so as to be selected substantially
10 simultaneously and said memory cells thus selected are connected to said input-output terminals in a one-to-one manner;

(b) a first switch circuit connected to said input-output terminals of said memory cell array and having
15 a plurality of control terminals, the first switch circuit being arranged to selectively connect a said input-output terminal to an input circuit in accordance with signals on the control terminals;

(c) a second switch circuit connected to said
20 input-output terminals of said memory cell array and having a plurality of control terminals, the second switch circuit being arranged to selectively connect a said input-output terminal to an output circuit in accordance with signals on the control terminals;

25 (d) a control circuit outputting a control signal; and

(e) a selecting circuit arranged to output to



said control terminals of said first and second switch circuits a selection signal which connects a predetermined input-output terminal of said plurality of input-output terminals of said memory cell array to said input and output circuits, and thereafter to output to said control terminals selection signals which connect sequentially and selectively a plurality of input-output terminals other than said predetermined input-output terminal to said input and output circuits in response to the control signal output from said control circuit.

15. A semiconductor memory device according to claim 14, wherein said selecting circuit comprises a second selecting circuit with a plurality of output terminals, said second selecting circuit outputting a plurality of predetermined second selection signals; and a shift register consisting of a plurality of registers receiving the control signals output from said control circuit and outputting said selection signals; said shift register outputting said selection signal which connects one of said plurality of input-output terminals of said memory cell array determined by said second selection signals to said input and output circuits and then outputting said selection signals which connect sequentially and selectively said input-output terminals to said input and output circuits every time said shift register is operated on by the control signal.



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16. A semiconductor memory device according to claim 15, further including a third selecting circuit outputting selection signals for selecting said plurality of memory cells from said memory cell array, and in which
5 said memory cells thus selected are connected to said input-output terminals of said memory cell array, thereby executing the writing or reading of data into or from said selected memory cells via said input-output terminals.

17. A semiconductor memory device according to
10 claim 16, wherein said third selecting circuit comprises a buffer circuit receiving a plurality of third address signals supplied at a first point in time and a plurality of fourth address signals supplied at a second point in time and outputting a plurality of third signals based on
15 said plurality of third address signals and a plurality of fourth signals based on said plurality of fourth address signals; and a decoder circuit receiving the plurality of said third and fourth signals and outputting selection signals for selecting said plurality of memory
20 cells from said memory cell array.

18. A semiconductor memory device according to claim 17, wherein said control circuit comprises a second control circuit having a first terminal to which a first control signal determining said first point in
25 time is applied and a second terminal to which a second control signal determining said second point in time is applied, and said second control circuit outputs said



control signal for operating said shift register when said first and second control signals are applied to said first and second terminals at a predetermined timing relationship, whereby said memory cells are selected sequentially from said plurality of memory cells selected from said memory cell array and are connected to said input and output circuits.

19. A semiconductor memory device according to claim 18, wherein said device is packaged in a package having a plurality of pins, said first terminal of said control circuit being connected to one of two pins of said plurality of pins and said second terminal of said control circuit being connected to the other of said two pins.

20. A semiconductor memory device according to any one of claims 14 to 19, wherein said first and second switch circuits consist of a plurality of gate circuits constituted by insulated gate field-effect transistors.

21. A semiconductor memory device according to any one of the preceding claims, wherein the number of said input-output terminals of said memory cell array is 4.

22. A semiconductor memory device according to claim 19, wherein said first terminal of said control circuit is connected to one of two pins of said plurality of pins other than that connected to said common terminal of said third selecting circuit, and said second terminal of said control circuit is connected to the other of said two pins.



23. A semiconductor memory device according to any one of the preceding claims, further including a plurality of amplifiers each of which latches the data read from a selected memory cell.

5 24. A semiconductor memory device according to any one of the preceding claims, wherein the data output through said output circuit is output serially by means of shift registers.

25. A semiconductor memory device including:

10 (a) a memory cell array having a plurality of input-output terminals, in which a plurality of memory cells are arranged so as to be selected substantially simultaneously and said memory cells thus selected are connected to said input-output terminals in a one-to-one
15 manner;

(b) a switch circuit connected to said input-output terminals of said memory cell array, and having a plurality of control terminals, the switch circuit being arranged to selectively connect a said input-output
20 terminal to an input circuit in accordance with signals on the control terminals;

(c) a control circuit outputting a control signal; and

(d) a selecting circuit arranged to receive
25 the control signal output from said control circuit and a plurality of signals corresponding to a plurality of address signals, and to apply a plurality of selection



signals to said control terminals of said switch circuit,
for first selectively connecting a predetermined one of
said input-output terminals to said input circuit and
for thereafter selectively and sequentially connecting
5 remaining input-output terminals other than said
predetermined one of said input-output terminals to
said input circuit.

26. A semiconductor memory device according to
claim 25, further including:

10 (e) a second selecting circuit having a
plurality of output terminals, said second selecting
circuit receiving the plurality of signals corresponding
to said address signals, and outputting a plurality of
second selection signals determined by said plurality of
15 signals thus received; and

(f) a shift register consisting of a plurality
of registers corresponding in a one-to-one manner to
said output terminals of said second selecting circuit,
said shift register receiving said second selection
20 signals applied via said output terminals corresponding
thereto and said control signals output from said control
circuit, and outputting selection signals which cause
the switch circuit to connect one of the input-output
terminals of said memory cell array determined by said
25 second selection signals to said input circuit, and then
outputting further such selection signals which cause
the switch circuit to selectively and sequentially connect





the other said input-output terminals of said memory cell array to said input circuit, every time said shift register is operated on by the control signal.

27. A semiconductor memory device according to
5 claim 26, wherein said second selecting circuit comprises a decoder circuit decoding the plurality of signals corresponding to the plurality of said address signals.

28. A semiconductor memory device according to
10 claim 27, wherein the plurality of said signals corresponding to said plurality of address signals which are applied to said second selecting circuit consist of first signals based on first address signals applied at a first point in time and second signals based on second address signals applied at a second point in time.

15 29. A semiconductor memory device according to claim 28, wherein said control circuit comprises a first terminal to which a first control signal determining said first point in time is applied, a second terminal to which a second control signal determining said second
20 point in time is applied, and a second control circuit outputting said control signal for operating said shift register when said first and second control signals are applied to said first and second terminals at a predetermined timing relationship, so that memory cells are
25 selected sequentially from said plurality of memory cells selected from said memory cell array and are connected to said input circuit.



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30. A semiconductor memory device according to claim 29, further including a third selecting circuit outputting selection signals for selecting said plurality of memory cells from said memory cell array, and in which
5 said memory cells thus selected are connected to said input-output terminals of said memory cell array, thereby executing the writing of data into said selected memory cells via said input-output terminals.

31. A semiconductor memory device as defined in
10 claim 30, wherein said third selecting circuit comprises: a first buffer circuit which receives a first address signal supplied at the first point in time and a second address signal applied at the second point in time and applies said first and second signals to said decoder
15 circuit; a second buffer circuit which receives a plurality of third address signals applied at said first point in time, and a plurality of fourth address signals supplied at said second point in time, and outputs a plurality of third signals based on said plurality of third address
20 signals and a plurality of fourth signals based on said plurality of fourth address signals; and a second decoder circuit which receives the plurality of said third and fourth signals and outputs selection signals for selecting said plurality of memory cells from said
25 memory cell array.



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32. A semiconductor memory device according to claim 31, wherein said third selecting circuit further includes a common terminal receiving said first address signal supplied at the first point in time and said second
5 address signal supplied at the second point in time, and in which said first and second address signals are applied from said common terminal to said first buffer circuit.

33. A semiconductor memory device according to claim 32, wherein said device is packaged in a package
10 having a plurality of pins and in which said common terminal of said third selecting circuit is connected to one of said plurality of pins.

34. A semiconductor memory device according to claim 33, wherein said pin to which said common terminal
15 of said third selecting circuit is connected is pin 1.

35. A semiconductor memory device according to any one of the preceding claims 25 to 34, wherein said memory cell array consists of a plurality of memory cell
matrices each containing a plurality of memory cells,
20 and each of said memory cell matrices has one of said plurality of input-output terminals.

36. A semiconductor memory device according to any one of the preceding claims 25 to 35, wherein said switch circuit consists of a plurality of gate circuits.

25 37. A semiconductor memory device according to any one of the preceding claims 28 to 34, wherein said selecting circuit comprises a latch circuit arranged to



latch said first signals and said second signals and to apply said latched first and second signals to said decoder circuit.

38. A semiconductor memory device according to claim 33, wherein said first terminal of said control circuit is connected to one of two pins of said plurality of pins other than that connected to said common terminal of said third selecting circuit, and said second terminal of said control circuit is connected to the other of said two pins.

39. A semiconductor memory device including:

(a) a memory cell array having a plurality of input-output terminals, in which a plurality of memory cells are arranged so as to be selected substantially simultaneously and said memory cells thus selected are connected to said input-output terminals in a one-to-one manner;

(b) a switch circuit connected to said input-output terminals of said memory cell array, and having a plurality of control terminals, the switch circuit being arranged to selectively connected a said input-output terminal to an output circuit in accordance with signals on the control terminals;

(c) a control circuit outputting a control signal; and

(d) a selecting circuit arranged to receive the control signal output from said control circuit and a plurality of signals corresponding to a plurality of



address signals, and to apply a plurality of selection signals to said control terminals of said switch circuit, for first selectively connecting a predetermined one of said input-output terminals to said output circuit and
5 for thereafter selectively and sequentially connecting remaining input output terminals other than said predetermined one of said input-output terminals to said output circuit.

40. A semiconductor memory device according to
10 claim 39, further including:

(e) a second selecting circuit with a plurality of output terminals, said second selecting circuit receiving the plurality of signals corresponding to said address signals, and outputting a plurality of second
15 selection signals determined by said plurality of signals thus received; and

(f) a shift register consisting of a plurality of registers corresponding in a one-to-one manner to said output terminals of said second selecting circuit,
20 said shift register receiving said second selection signals applied via said output terminals corresponding thereto and said control signals output from said control circuit, and outputting selection signals which cause the switch circuit to connect one of the input-output terminals
25 of said memory cell array determined by said second selection signals to said output circuit, and then outputting further such selection signals which cause



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the switch circuit to selectively and sequentially connect the other said input-output terminals of said memory cell array to said output circuit, every time said shift register is operated on by the control signal.

5 41. A semiconductor memory device according to claim 40, wherein said second selecting circuit comprises a decoder circuit decoding the plurality of signals corresponding to the plurality of said address signals.

42. A semiconductor memory device according to
10 claim 41, wherein the plurality of said signals corresponding to said plurality of address signals which are applied to said second selecting circuit consist of first signals based on first address signals applied at a first point in time and second signals based on second address
15 signals applied at a second point in time.

43. A semiconductor memory device according to claim 42, wherein said control circuit comprises a first terminal to which a first control signal determining said first point in time is applied, a second terminal to
20 which a second control signal determining said second point in time is applied, and a second control circuit outputting said control signal for operating said shift register when said first and second control signals are applied to said first and second terminals at a
25 predetermined timing relationship, so that memory cells are selected sequentially from said plurality of memory cells selected from said memory cell array and are connected to said output circuit.



44. A semiconductor memory device according to claim 43, further including a third selecting circuit outputting selection signals for selecting said plurality of memory cells from said memory cell array, and in which
5 said memory cells thus selected are connected to said input-output terminals of said memory cell array, thereby executing the reading of data from said selected memory cells via said input-output terminals.

45. A semiconductor memory device according to
10 claim 44, wherein said third selecting circuit comprises: a first buffer circuit which receives a first address signal supplied at the first point in time and a second address signal applied at the second point in time and applies said first and second signals to said decoder
15 circuit; a second buffer circuit which receives a plurality of third address signals applied at said first point in time, and a plurality of fourth address signals supplied at said second point in time, and outputs a plurality of third signals based on said plurality of third address
20 signals and a plurality of fourth signals based on said plurality of fourth address signals; and a second decoder circuit which receives the plurality of said third and fourth signals and outputs selection signals for selecting said plurality of memory cells from said memory cell array.

25 46. A semiconductor memory device according to claim 45, wherein said third selecting circuit further comprises a common terminal receiving said first address



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signal supplied at the first point in time and said second address signal supplied at the second point in time, and in which said first and second address signals are applied from said common terminal to said first buffer circuit.

5 47. A semiconductor memory device according to claim 46, wherein said device is packaged in a package having a plurality of pins and in which said common terminal of said third selecting circuit is connected to one of said plurality of pins.

10 48. A semiconductor memory device according to claim 47, wherein said pin to which said common terminal of said third selecting circuit is connected is pin 1.

49. A semiconductor memory device according to any one of the preceding claims 39 to 48, wherein said memory
15 cell array consists of a plurality of memory cell matrices each containing a plurality of memory cells, and each of said memory cell matrices has one of said plurality of input-output terminals.

50. A semiconductor memory device according to any
20 one of the preceding claims 39 to 49, wherein said switch circuit consists of a plurality of gate circuits.

51. A semiconductor memory device according to any one of the preceding claims 42 to 48, wherein said selecting circuit comprises a latch circuit arranged to
25 latch said first signals and said second signals and to apply said latched first and second signals to said decoder circuit.



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52. A semiconductor memory device according to claim 47, wherein said first terminal of said control circuit is connected to one of two pins of said plurality of pins other than that connected to said common terminal of said third selecting circuit, and said second terminal of said control circuit is connected to the other of said two pins.

53. A semiconductor memory device constructed substantially as herein described with reference to and 10 as illustrated in the accompanying drawings.



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