

CLAIMS:

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1. Arrangement for generating digital signals (a..i) for a transmission system, more specifically control signals (a..i) recurring, in essence, in a predeterminable time frame, characterized in that the arrangement (103) for generating the digital signals (a..i) comprises a write/read memory (11) for storing signal variations
5 of the digital signals, an addressing arrangement (12) allocated to the write/read memory (11) for selecting the digital signals (a..i).
2. Arrangement as claimed in Claim 1, characterized in that the arrangement (103) for generating the digital signals (a..i) comprises a comparator (14) for comparing the content of a comparative counter (13) specifically clocked with a multiple of a clock
10 of the digital signals (a..i) with the content of a time Table (T) which can be stored in the write/read memory (11).
3. Arrangement as claimed in one of the Claims 1 or 2, characterized in that the arrangement (103) for generating the digital signals (a..i) comprises synchronizing means (19, 23) for synchronizing the time frames of the digital signals with a
15 predeterminable time frame and/or for synchronizing for a predeterminable time slot a first time frame with a further time frame asynchronous thereto, while the reference to the first time frame is maintained.
4. Arrangement as claimed in one of the Claims 1 to 3, characterized in that the area of the write/read memory (11) which area is provided for storing the digital
20 signals (a..i) is subdivided into at least two separately selectable sub-areas.
5. Arrangement as claimed in one of the Claims 1 to 4, characterized in that at least one interrupt signal is stored in the write/read memory (11).
6. Arrangement as claimed in one of the Claims 1 to 5, characterized in that the arrangement is realised as an integrated semiconductor circuit or as an integrated
25 peripheral function on a microprocessor.
7. Arrangement as claimed in one of the Claims 1 to 6, characterized in that the digital signals are provided for controlling a radio transceiver (100a, 100b, 101) of a radio transmission system.

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8. Arrangement as claimed in one of the Claims 1 to 7, characterized in that the radio transmission system is a mobile radio system and in that the arrangement is integrated in a mobile station (100) and/or base station (101) of the mobile radio system.
- 5 9. Arrangement as claimed in one of the Claims 1 to 8, characterized in that the arrangement is provided for a mobile station and/or base station of a radio transmission system which operates according to a time-division multiple access method.
10. Radio transceiver (100, 101) comprising an arrangement (103) as claimed
- 10 in one of the Claims 1 to 9.

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DESCRIPTION

Arrangement for generating digital signals.

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The invention relates to an arrangement for generating digital signals for a transmission system, more specifically control signals recurring, in essence, in a predeterminable time frame.

Such an arrangement is necessary, for example, in transmitters and
5 receivers (radio sets) for the present Pan-European mobile radio system. In this mobile radio system speech signals are transmitted in digitized form together with other digital signals in a time-division multiple access method (TDMA). This requires a precise time control of various functions. A multiplicity of control signals is necessary for this purpose, which signals generally exhibit a periodic variation, that is, are cyclically
10 recurrent in a predeterminable time frame. In addition, these control signals should also be individually controllable in dependence on a large number of different operating requirements. The control signals may be derived from the signal of a central clock generator designated as a timer. This clock generator is in essence based on a counter which triggers an interrupt function of the processor of the radio set when a
15 predetermined value is reached or exceeded and/or directly affects external control signals. If a large number of control signals are generated in this manner with a rather high time-dependent resolution, the processor is loaded very heavily. Another possibility consists of generating the control signals by means of specific switch mechanisms. The control signals are predetermined, so that considerable restrictions arise with respect to
20 the flexibility when these switch mechanisms are used, for example, when individual control signals are changed.

It is an object of the invention to provide an arrangement of the type mentioned in the opening paragraph which makes it possible to generate in a simple manner a multiplicity of digital signals which have a high time-dependent resolution and
25 flexibility when used.

This object is achieved with an arrangement of the type mentioned in the opening paragraph, in that the arrangement for generating the digital signals comprises a write/read memory for storing signal variations with time of the digital signals, and an addressing arrangement allocated to the write/read memory for selecting the digital

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signals.

The storage capacity of the write/read memory then determines the number as well as the complexity of the digital signals (= control signals). An addressing arrangement, for example, an address counter selects the control signals, that is, a specific state of all the control signals, which address counter identifies this state with the aid of an address assigned in the write/read memory. The control signal generation thus only asks for the activation, that is, the selection of the individual control signals, so that the loading of the allocated processor is minimized. Furthermore, the simple indication of each address by individual control signals provides a complete freedom of choice of the order of the control signals. In addition, by simply overwriting control signals stored so far, the write/read memory makes it possible to feed new signal variations of a control signal.

A high time-dependent resolution of the digital signals is provided in that the arrangement for generating digital signals comprises a comparator for comparing the content of a comparative counter specifically clocked with a multiple of a clock of the digital signals with the content of a time Table that can be stored in the write/read memory. If the comparative counter operates as a so-called quarter bit counter, for example, with four times the bit clock of the control signals, there is a control signal resolution into quarter bits. The time Table of the write/read memory may then list for each control signal all the time frame start instants possible with this resolution. A certain state of the control signals is thus not selected until both the address of the address counter matches the predetermined address and the start instant information contained in the time Table matches the predetermined start instant.

In a radio transceiver operating according to a time-division multiple access method, a synchronization of the digital signals may be effected in that the arrangement for generating the digital signals comprises synchronizing means for synchronizing the time frame of the digital signals with a predeterminable time frame and/or for synchronizing a predeterminable time interval of a first time frame with a further time frame asynchronous thereto, while the reference to the first time frame is maintained. If, for example, during the operation of a mobile radio telephone the signal delay of the control signals is changed, the control signals (= digital signals) may again be synchronized with the predeterminable time frame, specifically the received time frame with the aid of the synchronizing means. This is effected, for example, by



inserting or omitting an additional clock of the comparative counter. With a cellular structure of a mobile radio system it is made possible to switch to and fro between the time frames of various, for example, adjacent radio cells, when the synchronizing means effect a synchronization of a first time frame with a further time frame

- 5 asynchronous thereto for a predeterminable time interval, while the reference to the first time frame is maintained.

If the write/read memory is subdivided into at least two separately selectable areas, there is a possibility of switching very rapidly between various types of operation, that is, between various control signal records. In addition, a part of the
10 write/read memory which is unused at a particular instant may be used by the processor without any problems with respect to time.

If at least one interrupt signal is stored in the write/read memory, an interruption may be predetermined with the aid of the interrupt signal for example once per time frame in accordance with a desired requirement. This makes it also possible to
15 switch to a different operating mode by means of other control signals stored in a second area of the write/read memory.

If the arrangement is realised as an integrated semiconductor circuit, especially in mobile radio telephones this provides the possibility of integrating in a space-saving manner the whole arrangement for generating the most diverse control
20 signals in a housing which has small outside dimensions. If the arrangement is realised as an integrated peripheral function on a microprocessor, for example, a microprocessor already available in a radio transceiver may at the same time incorporate the whole control signal generating arrangement.

A simple presentation of digital signals, especially for a mobile radio
25 system operating according to a time-division multiple access method is made possible in that the digital signals are available for controlling a radio transceiver of a radio transmission system.

If the digital transmission system is a mobile radio system and the arrangement in a mobile and/or base station of the digital mobile radio system are
30 integrated, the given requirements, for example, for the Pan-European mobile radio system may be satisfied with an arrangement of this type.

The invention will be further explained in the following with reference to

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the exemplary embodiments represented in the drawing Figures, in which:

Fig. 1 shows a simplified block diagram of an arrangement for generating control signals;

Fig. 2 shows the variations of various control signals;

5 Fig. 3 shows a block diagram of an arrangement for generating control signals;

Fig. 4 shows a radio transceiver; and

Fig. 5 shows a cellularly structured mobile radio system.

10 The block diagram represented in Fig. 1 shows an exemplary embodiment for an arrangement for generating digital signals. These digital signals may be, for example, control signals for the various functions (*e.g.* transmitter, receiver) of a digital radio transmission system, which are recurrent in time frames which frames comprise a plurality of time slots. This is the manner of operation of, for example, radio sets
15 operated according to the time-division multiple access method (TDMA), and are necessary, for example, for the future Pan-European mobile radio system GSM (Groupe Spéciale Mobile). A precise time control of a plurality of functions is then required. This is effected with a plurality of control signals which generally exhibit a periodic behaviour, but for which it is also necessary to influence them individually depending
20 on a large number of different requirements. For this purpose, the control signals in the exemplary embodiment shown in Fig. 1 are stored in a write/read memory 11. The write/read memory 11 is subdivided into a time Table T, signal Tables RX, TX, a pulse Table P as well as an interrupt Table I. The content of the time Table T is compared to the content of a comparative counter 13 by means of a comparator 14. The comparative
25 counter 13 is clocked with a clock t corresponding to a multiple of the clock of the control signals. In the event of matching values the appropriate control signal is selected from the signal Tables RX, TX over a control line S by way of an address counter 12 and an address decoder A included in the write/read memory 11. In addition, the control line S is connected to buffers 15, 16, 17, 18. By way of these buffers 15 to 18
30 the information signals read from the signal Tables RX, TX, from the pulse Table P and from the interrupt Table I are presented as signals SR, ST, SP and SI.

The central element of the exemplary embodiment represented in Fig. 1 of an arrangement for regenerating time-dependent functions is formed by the write/read



memory 11. Each line of the write/read memory 11 is subdivided into five areas and has a specific control signal code in the information signals. In the area of the time Table T each line stores the exact start instant of the control signal accommodated on the same line in the areas of the signal Tables RX, TX. For example, if the clock t of the comparative counter 13 is four times the bit clock of the control signal, four start instants are possible for each control signal during each bit period of the predetermined time frame. The area of the signal Table RX accommodates, for example, all the control signals relating to the receiver, and the area of the signal Table TX accommodates the control signals relating to the transmitter. The area of the pulse Table P accommodates information signals for triggering synchronizing signals, which synchronizing signals generate a pulse in each output line for example for synchronization of the control signals. Furthermore, a synchronization of the time frame of the control signals with the received time frame may be effected by means of the pulse Table P. A further possibility consists of the fact that a synchronization may temporarily be effected between the time frame of the control signals and a further time frame asynchronous relative to the predetermined time frame, without the reference to the predetermined time frame being lost. The content of the interrupt Table I may be transported by way of the buffer 18 to, for example, an interrupt generator (not shown in Fig. 1).

The operation of the arrangement represented in Fig. 1 is thus in essence effected in the following steps. The content, for example, of the first line of the time Table T is compared with the content of the comparative counter 13 by means of the comparator 14. The comparative counter 13 is clocked, for example, with four times the time frame clock and continuously incremented with this clock. The period of the comparative counter thus exactly corresponds to a time frame. If the comparator 14 detects equality between the content of the comparative counter 13 and the content of the time Table T, the following operations are executed.

The contents of the signal Tables RX, TX are loaded in the buffers 15, 16, and presented as control signals SR, ST at the outputs. The information signals contained in the pulse Table are loaded in the buffer 17 and transported as a control signal SP, for example, to an arrangement (not shown in Fig. 1) which generates a pulse on each output line. For example, a pulse is only generated when the appropriate content is a logic "1", otherwise no reaction will follow. The pulse length is then, for



example, $1/8$ bit. The content of the interrupt Table I is transported, for example, to an interrupt generator (not shown in Fig. 1), which activates, for example, an interrupt line to a host processor. Once this procedure has been terminated, the comparative counter 13 is incremented. This causes a new time value to appear in the comparator 14. When
5 the comparative counter has reached this time value, the above-described procedures are rerun.

The structure represented in Fig. 1 makes it thus possible for said values having a quarter bit resolution at random instants in the predetermined time frame to switch one or various control signals on or off, generate one or more different pulses or
10 generate an interrupt. These functions may also be combined at random. For this purpose it is only necessary that the "results", that is, the information stored in the write/read memory, be stored in a sorted manner in the order in which they occur, that is, according to enhancing values of the time Table T. The arrangement represented in Fig. 1 thus enables the generation of a random number of control signals with a high
15 time-dependent resolution and flexibility of the generated control signals while at the same time the loading of the host processor is minimized. A still more flexible operation of the arrangement shown in Fig. 1 may be achieved in that the write/read memory 11 and the associated time Table T, the signal Tables RX, TX as well as the pulse and interrupt Tables P and I respectively, are subdivided into a plurality of
20 independent sections. Each section of the write/read memory 11 is then activated by means of an information signal that can be given to the address counter 12 by the host processor. As a result, it is possible to switch the arrangement very rapidly between two different types of operation by means of optionally different control signals. In addition, a just unused Table section may be used without time problems by the host processor.

25 Fig. 2 shows an embodiment for control signals a to i to be generated. Minimum requirements for realising such control signals are that, on the one hand, the necessary control signals are generated largely independently while the utilization of the host processor is minimized, and on the other hand, a high degree of flexibility, for example in respect of the start instant of the control signals is to be guaranteed for
30 making adaptations possible to different set configurations of a mobile radio system. Such a flexibility ensures the applicability in later generations of sets, or makes the use of such an arrangement structured as an integrated semiconductor circuit possible also in sets made by other manufacturers.



The signal variations a to i shown in Fig. 2 are recurrent in a time frame subdivided into seven time slots 0 to 7. The signals a to f are, for example, the control signals stored in the signal Tables RX, TX of the arrangement shown in Fig. 1, whereas the signals g to i, for example, represent synchronizing or interrupt signals respectively stored in the pulse Table P or interrupt Table I respectively (Fig. 1). The double-pointed arrow A at the beginning of the first time window of the time frame symbolizes that the total time frame can be synchronized with the received time frame by means of the arrangement shown in Fig. 1. The arrow denoted B symbolizes the possibility of correcting once per time frame deviations caused by signal delays. This is effected, for example, by omitting or inserting an additional clock at the request of the host processor. This swallow-insert function shortens or lengthens the time frame by a quarter bit. The subsequent time frames are shifted accordingly.

In an arrangement provided for the future Pan-European mobile radio system (GSM = Groupe Spéciale Mobile), the signals represented in Fig. 2 carry out, for example, the following tasks:

- Preparation of signals for controlling the time-division multiple access method;
- Controlling the signal processor for the baseband processing;
- Controlling the software of a digital signal processor; and
- Taking over all the hardware control and monitoring tasks.

Fig. 3 shows a detailed block diagram of an arrangement for generating control signals. Like reference numerals are used for the blocks already represented in connection with Fig. 1. The central element is here again the write/read memory 11 which is subdivided into the time Table T, the signal Tables RX, TX as well as the pulse Table P and the interrupt Table I. All the clock signals necessary in the arrangement shown in Fig. 3 are derived from an input clock cl. For example, for digitizing the audio signal, a clock sp is derived with the aid of a clock divider T5. Multiples of the input clock cl may be derived by means of clock dividers T1, T2, T3. These multiples of the input clock are applied to a multiplexer 30 from whose output a desired bit clock tn may be tapped. A further clock divider T4 is arranged in series with the clock dividers T1, T2, T3 and produces a bit clock tbit. As already observed with respect to Fig. 1, the comparative counter 13 is clocked with a clock t which is a multiple of the clock tbit of the control signals. In addition to the exemplary embodiment shown in Fig. 1, an offset adder 19 is inserted between the comparative



counter 13 and the comparator 14 in the arrangement shown in Fig. 3. The arrangement may be connected to the host processor over a data bus HI by way of 12 registers R1 to R12. The control signals SR, ST, SP are presented by way of output registers 20, 21, 22.

5 The offset adder 19 makes a shift of the time frame relative to the time frame of an adjacent cell in a mobile radio transmission system possible. A processor (host interface) connected by way of a control bus HI then computes the offset relative to the so-called serving station (serving cell). This offset may be caused by delays. The offset adder 19 adds the complement of the thus determined offset to the content of the
10 comparative counter 13 *via* a buffer 23. The result of this addition forms the input signal for the comparator 14. A further operation is necessary to deal with the offset, because the address counter 12 generally indicates an erroneous Table entry in the time Table T after the value in the offset buffer 23 has changed. For this reason it is necessary to correct the address counter 12, because otherwise in the worst case a
15 whole time frame may be lost as a result of the change of the offset. For this purpose, the address counter 12 is reset after each change of the content of the offset register R4. The address counter 12 is incremented as long as the Table entries belonging to the content of the address counter 12 in the time Table T are smaller than the value at the output of the offset adder 19. The contents of the sections RX, TX, P, I of the
20 write/read memory 11 are then ignored, that is, the outputs remain unchanged and no synchronizing pulses or interrupts are produced. As a result, the address counter 12 points at the first Table entry of the time Table T that exceeds the instantaneous count of the sum of the content of the comparative counter 13 and the offset. This method ensures that the address counter 12 is corrected in the fastest way possible and the
25 output states directly change from the old to the new state. By way of a signal FI (Frame Interrupt) consisting, for example, of a pulse 1/8 bit in length, once the offset register R4 has been loaded, the beginning of the first time frame may be marked by a correct setting of the comparative counter 13.

 The processor gains access to twelve registers (R1 to R12) over the
30 connection HI arranged as a data bus. For example, the synchronization or the selection of the desired bit clock is verified by way of the control register R12. The register R5 is the address register for accessing the time Table. This register may identify which line of the time Table T is written or read out by means of a write/read access to a



register (R6 to R10).

The registers R6 to R10 form temporary registers for writing/reading the individual sections of the time Table T. As already observed, the register R4 forms the time offset register. The registers R1 to R3 form the mask register. For example, a "0" recorded in this register may keep the corresponding signal line at "0". The register R11 forms the interrupt vector register. A control function 24 coordinates all the operations in the arrangement shown in Fig. 3. The control signals SR, ST, SP are finally supplied by way of the output registers 20, 21, 22 respectively.

Fig. 4 shows a diagrammatic structure of a radio transceiver 100, 101 comprising an arrangement 103 for generating control signals a, b, c, d. The radio transceiver 100, 101 comprises a diplexer 107 which has an aerial. The diplexer 107 is connected to a transmitter 104 and a receiver 102. The transmitter 104 is connected to a microphone 110, for example of a handset 117, by way of a modulator 109. The handset 117 further includes a loudspeaker 114 which is connected to the receiver 102 by way of a demodulator 113. The transmitter 104 and the receiver 102 are driven by a frequency generator 111 to which a control signal i is applied. The radio transceiver 100, 101 additionally includes a control unit 115 connected to the modulator 109, to the demodulator 113 and also to the arrangement 103 for generating the control signals. Furthermore, a clock generator 116 is provided which applies a clock t to the control unit 115 and also to the arrangement 103 for generating the control signals. The arrangement 103 for generating the control signals and the control unit 115 are interconnected by way of a line HI.

The radio transceiver 100, 101 shown in Fig. 4 operates according to a time-division multiple access method (TDMA) and is to be used, for example, in the Pan-European mobile radio system GSM. This requires an exact time-dependent control of the operations of the transmitter 104 and the receiver 102 and of the frequency generator 111. This control is effected with the aid of control signals a..i, generated with the aid of the arrangement 103. The generation of the control signals a..i is explained with reference to the Figs. 1 to 3.

Fig. 5 shows a cellular arrangement of a mobile radio system. It comprises base stations 100a, 100b as well as mobile stations 101. The mobile stations 101 are, for example, mobile radio telephones in a private car, a train and so on, or structured as mobile handsets. The mobile radio system consists of separate radio cells

105a, 105b, 105c, 105d, while only the range boundaries are shown of radio cells 105c, 105d. Each base station 100a, 100b as well as each mobile station 101 comprises, for example, a transmitter arrangement 102 as well as a receiver arrangement 104. The transmitter arrangement 102 and receiver arrangement 104 make the transmission
5 possible of radio signals between base station 100a, 100b and the mobile stations 101. For this purpose an aerial is allocated to each base station 100a, 100b and mobile station 101. In addition, each base station 100a, 100b and mobile station 101 comprises an arrangement for generating control signals 103.

In the mobile radio transmission system represented in Fig. 5, for
10 example, the Pan-European mobile radio system GSM is discussed in which control signals are necessary which are recurrent in a time frame consisting of one or more time slots. The control signals control the various functions, more specifically, that of the transmitter arrangement 102 and the receiver arrangement 104. The control signals generated with the aid of the arrangement 103 in addition carry out the following tasks:
15 preparation of signals for controlling the time-division multiple access method, controlling with time the processor for the baseband processing, and controlling the software of a digital host processor. The arrangement 103 comprises a write/read memory as has already been described with reference to the Figs. 1 and 3, while the selection of the control signals is effected by means of the addressing arrangements
20 allocated to the write/read memory. The arrangement 103 comprises a synchronizing means which, for a predeterminable time slot, makes a synchronization possible of a first time frame produced, for example, by the radio cell 105a, with another time frame asynchronous thereto which is produced, for example, by the radio cell 105b. During this operation the reference to the first time frame of the radio cell 105a is maintained,
25 so that it is possible in the cellularly structured mobile radio system as shown in Fig. 5 to switch to and fro between the time frames of adjacent radio cells 105a and 105b.

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