

SPECIFICATION

CARRIER FOR DOUBLE-SIDE POLISHING APPARATUS, DOUBLE-SIDE POLISHING APPARATUS USING THE SAME, AND DOUBLE-SIDE POLISHING METHOD

TECHNICAL FIELD

[0001]

The present invention relates to a carrier for double-side polishing apparatus that holds a semiconductor wafer when polishing the semiconductor wafer in a double-side polishing apparatus.

BACKGROUND ART

[0002]

When, e.g., polishing both surfaces of a semiconductor wafer, the semiconductor wafer is held by a carrier in conventional examples. This carrier is formed with a thickness thinner than that of the semiconductor wafer and has a wafer holding hole through which the wafer is held at a predetermined position between an upper turn table and a lower turn table of a double-side polishing apparatus. The semiconductor wafer is inserted into and held in this wafer holding hole, upper and lower surfaces of the semiconductor wafer are sandwiched by polishing jig, e.g., polishing pads provided on opposed surfaces of the upper turn table and the lower turn table, and polishing is carried out while

supplying a polishing agent to the polishing target surfaces.

[0003]

When double-side polishing is carried out in this manner, an outer peripheral portion alone of the semiconductor wafer is excessively polished due to, e.g., concentration of a pressure on the outer peripheral portion of the semiconductor wafer or an influence of viscoelasticity of a polishing slurry or polishing pads, and peripheral sag occurs. There is a problem that this peripheral sag degrades a flatness of the wafer.

[0004]

As a method for reducing such peripheral sag, there is disclosed a method for performing a secondary double-side polishing step that remedies peripheral sag produced at a primary double-side polishing step (see Japanese Unexamined Patent Publication (Kokai) No. 2005-158798).

However, this method has a defect that the number of steps is increased when the secondary double-side polishing step that remedies the peripheral sag is performed, and a double-side polishing method that can more readily reduce the peripheral sag has been demanded.

[0005]

Further, in conventional wafer polishing, dressing of polishing pad surfaces is performed by using, e.g., a ceramic plate in order to obtain stable polishing characteristics. However, in the double-side polishing,

not only the wafer as a workpiece but also a carrier is in contact with the polishing pads, an effect of dressing of the polishing pad surfaces does not last long, and there is a problem that dressing of the polishing pad surfaces must be frequently carried out by using, e.g., a ceramic plate.

Furthermore, there is also a problem that a life of the carrier itself is short and a cost is increased.

DISCLOSURE OF INVENTION

[0006]

Therefore, in view of the above-explained problems, it is an object of the present invention to provide a carrier for double-side polishing apparatus that enables stably and efficiently producing a high-quality wafer having a high flatness with reduced wafer peripheral sag at a low cost at the time of double-side polishing of the semiconductor wafer, a double-side polishing apparatus using the same, and a double-side polishing method.

[0007]

To achieve this object, according to the present invention, there is provided a carrier for double-side polishing apparatus which is set between upper and lower turn tables having polishing pads attached thereto and has a holding hole in which a semiconductor wafer sandwiched between the upper and lower turn tables is held at the time of polishing in a double-side polishing apparatus, wherein a material of the carrier is titanium, and surface

roughness of the titanium carrier is 0.14 μm or above in terms of Ra.

[0008]

When the material of the carrier is titanium, since a hardness is higher and abrasion at the time of polishing is smaller than those of a resin, a carrier life can be improved. Furthermore, titanium itself has a small diffusion coefficient in the semiconductor wafer, e.g., silicon, it hardly becomes a problem as an impurity, and a metal impurity having a large diffusion coefficient like Fe is not present in titanium, thereby suppressing contamination of the metal impurity with respect to the semiconductor wafer. Moreover, when such a titanium carrier having surface roughness of 0.14 μm or above in terms of Ra is used, the high-quality wafer having reduced peripheral sag and a high flatness can be stably efficiently produced. Additionally, since dressing of the polishing pads can be performed by using the carrier surface during polishing, a frequency of dressing of the polishing pads using, e.g., ceramic plate can be reduced, thus efficient polishing can be performed.

[0009]

At this time, it is preferable for the surface roughness to be 0.32 μm or above in terms of Ra.

When the surface roughness of the carrier is 0.32 μm or above in terms of Ra, the high-quality wafer having reduced peripheral sag and a high flatness can be produced.

[0010]

Moreover, it is preferable that the carrier to have grooves each reaching the holding hole from a carrier outer peripheral side on front and back surfaces thereof.

[0011]

When the carrier has the grooves each reaching the holding hole from the carrier outer peripheral side on front and back surfaces thereof in this manner, since the polishing liquid is supplied to the semiconductor wafer through the grooves at the time of polishing, a resistance undergone by the wafer outer peripheral portion at the time of polishing can be alleviated, and the peripheral sag can be reduced. Additionally, dressing of the polishing pads can be also performed by the groove during polishing, a frequency of dressing of the polishing pads using, e.g., ceramic plate can be further decreased.

[0012]

Further, a pattern of the grooves can be a grid-like pattern or a radial pattern.

When the pattern of the grooves is the grid-like pattern or the radial pattern in this manner, the polishing liquid can be easily and assuredly supplied to the semiconductor wafer at the time of polishing.

[0013]

Furthermore, when a double-side polishing apparatus comprising at least the carrier for double-side polishing apparatus according to the present invention is provided,

since the material of the carrier is titanium, a life can be increased, and contamination of a metal impurity with respect to a semiconductor wafer can be suppressed, thereby producing the high-quality wafer having reduced peripheral sag and a high flatness. Moreover, since dressing of polishing pads can be performed by carrier surfaces during polishing, a frequency of dressing of the polishing pads using, e.g., ceramic plate can be reduced, thus considerably improving an operating rate of the apparatus.

[0014]

Furthermore, there is provided a double-side polishing method for a semiconductor wafer, comprising: arranging the carrier between upper and lower turn tables holding the semiconductor wafer in a holding hole formed in the carrier; and sandwiching the semiconductor wafer between the upper and lower turn tables to perform double-side polishing.

[0015]

When the semiconductor wafer is held in the holding hole of the carrier for double-side polishing apparatus and sandwiched between the upper and lower turn tables to perform double-side polishing in this manner, a life of the carrier is increased, and the high-quality wafer having reduced contamination due to a metal impurity, decreased peripheral sag and a high flatness can be produced. Moreover, dressing of the polishing pads using the carrier surfaces can be carried out during polishing. Therefore, a

frequency of dressing of the polishing pads using, e.g., ceramic plate can be reduced, a cost can be decreased, and the semiconductor wafer can be efficiently subjected to double-side polishing.

[0016]

As explained above, according to the present invention, since titanium is adopted as the material, the carrier for double-side polishing apparatus that has an improved life and hardly occurs contamination due to a metal impurity can be provided, and the high-quality wafer having reduced contamination due to the metal impurity, and decreased peripheral sag, and a high flatness can be stably efficiently produced by using this carrier. Moreover, since dressing of the polishing pads can be performed by using the carrier surfaces during polishing, a frequency of dressing of the polishing pads using, e.g., a ceramic plate can be reduced. Therefore, a cost can be reduced, and the semiconductor wafer can be efficiently subjected to double-side polishing.

BRIEF DESCRIPTION OF DRAWINGS

[0017]

FIG. 1 is a vertical cross-sectional view showing an example of a double-side polishing apparatus including a carrier for double-side apparatus according to the present invention;

FIG. 2 is an internal structural view of the double-

side polishing apparatus as seen from a plane;

FIG. 3 is a schematic view showing a measurement position for a peripheral sag amount;

FIG. 4 shows measurement results of experiments;

FIG. 5 shows measurement results of experiments;

FIGS. 6 show an example of a pattern of grooves on front and back surfaces of the carrier for double-side polishing apparatus according to the present invention, (a) grid-like pattern, (b) radial pattern;

FIG. 7 shows measurement results of Examples 1 and 2 and Comparative Examples 1 and 2;

FIG. 8 shows measurement results of Examples 3 to 7; and

FIG. 9 shows measurement results of Example 8 and Comparative Example 3.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

[0018]

An embodiment according to the present invention will now be explained hereinafter, the present invention is not restricted thereto.

As a conventional carrier for double-side polishing apparatus, there is one formed of a metal, e.g., stainless or one having ceramic abrasive grains deposited on a surface of a metal plate, for example. However, when such carriers are used, an outer peripheral portion alone of a held semiconductor wafer is excessively polished at the

time of polishing to cause peripheral sag, or deposited abrasive grains fall off to produce scratches on a wafer surface, resulting in a problem that a quality of the semiconductor wafer is reduced.

[0019]

Further, in double-side polishing, there is a problem that an effect of dressing of polishing pad surfaces does not last long and a ceramic plate or the like must be frequently used to perform dressing of the polishing pad surfaces.

[0020]

Thus, as a result of keenly conducting experiments, the present inventor has found that a carrier for double-side polishing apparatus in which a material of the carrier is titanium and surface roughness of the titanium carrier is $0.14\text{ }\mu\text{m}$ or above in terms of Ra can solve the above-explained problem, thereby bringing the present invention to completion.

[0021]

That is, when such a carrier for double-side polishing apparatus is used to perform double-side polishing, a high-quality wafer having reduced peripheral sag and a high flatness can be produced. Furthermore, since dressing of the polishing pads can be performed by using carrier surfaces during polishing, a frequency of dressing of the polishing pads using, e.g., ceramic plate can be reduced, and polishing can be efficiently carried out. Moreover,

this carrier has a structure where each carrier surface itself is roughened without depositing abrasive grains, the abrasive grains do not fall off to produce scratches on the wafer surfaces. Additionally, since titanium is adopted as the material, a life becomes long, and contamination of, e.g., iron that affects a wafer quality does not occur.

[0022]

An embodiment according to the present invention will now be explained hereinafter with reference to appended drawings.

Here, FIG. 1 is a vertical cross-sectional view showing an example of a double-side polishing apparatus including a double-side polishing apparatus according to the present invention, and FIG. 2 is an internal structural view of the double-side polishing apparatus as seen from a plane.

[0023]

The present invention relates to an improvement in a carrier that holds a semiconductor wafer in a double-side polishing apparatus that simultaneously polishes both surfaces of the semiconductor wafer, and an outline of the double-side polishing apparatus will be first explained with reference to FIGS. 1 and 2.

[0024]

A double-side polishing apparatus 11 provided with a carrier 10 for double-side polishing apparatus includes a lower turn table 12 and an upper turn table 13 vertically

provided to face each other, and polishing pads 14 are attached to opposed surfaces sides of the respective turn tables 12 and 13. Further, a sun gear 15 is provided at a central portion between the upper turntable 13 and the lower turntable 12, and an internal gear 16 is provided at a rim portion. A semiconductor wafer W is held in a holding hole 17 of the carrier 10 and sandwiched between the upper turntable 13 and the lower turn table 12.

[0025]

Outer peripheral teeth of each carrier 10 mesh with respective tooth portions of the sun gear 15 and the internal gear 16, and each carrier 10 rotates around the sun gear 15 while rotating on its axis when the upper turn table 13 and the lower turn table 12 are rotated by a non-illustrated driving source. At this time, each semiconductor wafer W is held in the holding hole 17 of the carrier 10, and both surfaces thereof are simultaneously polished by the upper and lower polishing pads 14. At the time of polishing, a polishing liquid is supplied from a non-illustrated nozzle.

[0026]

It is to be noted that each carrier holds one wafer to perform polishing in FIG. 2, but carriers each having a number of holding holes may be used and a number of wafers may be held in each carrier to perform polishing.

[0027]

The carrier 10 for double-side polishing apparatus

according to the present invention set in the double-side polishing apparatus 11 will now be explained hereinafter.

A material of the carrier 10 according to the present invention is titanium, and this material has a higher hardness than that a SUS material coated with resin and does not have an impurity with a large diffusion coefficient like Fe or Ni contained therein. Therefore, scratches or damages can be reduced to increase a carrier life, and a cost can be reduced. Furthermore, contamination of a metal that becomes a problem of the semiconductor wafer W can be suppressed.

[0028]

A hardness of SUS as a conventional carrier material is 420 Hv, and a hardness of Ti as a material of the carrier 10 according to the present invention is 220 Hv. Therefore, it has been conventionally considered that Ti has the hardness lower than that of SUS and cannot be used as a material of the carrier. However, as explained above, a carrier having the exposed SUS material causes occurrence of crucial metal contamination with respect to the semiconductor wafer W, and the SUS material must be actually coated with a resin in order to suppress the metal contamination. Therefore, each surface of the carrier 10 according to the present invention is titanium, as its material is harder than each surface of the conventional carrier coated with a resin. Therefore, its life becomes long.

[0029]

Moreover, the carrier 10 according to the present invention is featured in that its surface roughness is 0.14 μm or above in terms of Ra. As a result of conducting the following experiment, the present inventor has discovered that the surface roughness of the carrier must be 0.14 μm or above in terms of Ra in order to obtain a wafer having reduced peripheral sag.

[0030]

(Experiment)

As the carrier for double-side polishing apparatus, a number of carriers which are formed of titanium and have different surface roughness degrees obtained by roughening front and back surfaces thereof by diamond pellets having different sizes were prepared.

The surface roughness of each carrier surface was measured by using Surf Test SJ-201P manufactured by Mitutoyo, and evaluation was carried out based on JIS B0601-1994.

[0031]

Each of the carriers was set in a double-side polishing apparatus, dressing of polishing pads was performed, and then double-side polishing of each silicon wafer having a diameter of 300 mm was performed. That is, the etched silicon wafer was set in each of five titanium carriers each having one holding hole, an upper turn table was rotated in a clockwise direction whilst a lower turn

table was rotated in a counterclockwise direction with a number of revolutions of 20 rpm and a load of 250 g/cm², and an alkaline solution containing colloidal silica was used as a polishing liquid to perform polishing.

[0032]

A peripheral sag amount of each polished wafer was measured. A wafer shape evaluation apparatus manufactured by Kuroda Precision Industries Ltd. was used to measure a difference in wafer shape between a position that is 1 mm away from a wafer edge and a position that is 3 mm away from the same as a peripheral sag amount with a section between a position that is 30 mm away from the wafer edge and a position where peripheral sag starts being determined as a reference plane as shown in FIG. 3. The following Table 1 and FIGS. 4 and 5 show measurement results.

[0033]

[Table 1]

Carrier surface roughness (Ra: μm)	Peripheral sag amount (μm)
0.03	0.162
0.08	0.154
0.14	0.099
0.24	0.068
0.32	0.059
0.50	0.061

[0034]

As is obvious from Table 1 and FIGS. 4 and 5, it can be understood that setting roughness of each carrier surface to 0.14 μm or above in terms of Ra enables

considerably improving the peripheral sag amount and obtaining each wafer having reduced peripheral sag and a high flatness. Further, it can be also understood that setting roughness of each carrier surface to 0.32 μm or above in terms of Ra enables further reducing the peripheral sag.

[0035]

It is to be noted that, in this experiment, deformation or damages of each carrier do not occur even if the front and back surfaces of the carrier are roughened, the carrier can be used to reach its life equivalent to that of a titanium carrier that is not subjected to processing of roughening the front and back surfaces of the carrier, and any difference in wafer quality other than a flatness from the non-processed carrier was not recognized.

However, when roughness of each carrier surface becomes too high, it can be considered that deformation or damages of the carrier are apt to occur and the life of the carrier is reduced. Therefore, it is desirable to set roughness of each surface to 10 μm or below in terms of Ra.

[0036]

Additionally, it has been revealed that dressing of the polishing pads can be performed during polishing by roughening the front and back surfaces of the carrier. Although dressing is performed once in 10 batches in conventional examples, the same effect can be obtained by carrying out dressing once in 40 batches.

[0037]

As explained above, the titanium carrier having surface roughness of 0.14 μm or above in terms of Ra, or more preferably the titanium carrier having surface roughness of 0.32 μm or above in terms of Ra has a long carrier life, and performing double-side polishing by using this carrier enables stably and efficiently producing a high-quality wafer having reduced metal contamination, decreased peripheral sag, and a high flatness at a low cost. Further, since dressing of the polishing pads can be performed by using carrier surfaces during polishing, a frequency of dressing of the polishing pads using, e.g., ceramic plate can be reduced, and an operating rate of the apparatus can be considerably improved.

[0038]

Furthermore, it is preferable for the carrier according to the present invention to have grooves each reaching the holding hole from the carrier outer peripheral side on the front and back surfaces thereof. When the carrier has such grooves, since the polishing liquid is supplied to the semiconductor wafer through the grooves at the time of polishing, a resistance undergone by the wafer outer peripheral portion at the time of polishing can be alleviated, thereby reducing the peripheral sag. Further, since dressing of the polishing pads can be carried out by using the grooves during polishing, a frequency of dressing of the polishing pads using, e.g., ceramic plate can be

further reduced.

[0039]

Although a pattern of the grooves is not restricted in particular, it may be, e.g., a grid-like pattern described in FIG. 6(a), a radial pattern grooves 18 shown in FIG. 6(b), or a pattern of horizontal stripes or vertical stripes.

Although a size of each groove 18 is not restricted in particular, the groove 18 may have, e.g., a width of 1 to 2 mm and a depth of 2 to 6 μm .

[0040]

It is to be noted that the planetary carrier for the double-side polishing apparatus has been taken as an example and explained, the carrier for double-side polishing apparatus according to the present invention is not restricted to the planetary type, and it is also effective to adopt a carrier for swinging type double-side polishing apparatus.

[0041]

When the double-side polishing apparatus 11 provided with the carrier 10 for the double-side polishing apparatus according to the present invention is adopted, a wafer having reduced metal contamination, decreased peripheral sag, and a high flatness can be obtained. Furthermore, since dressing of the polishing pads can be performed by using the carrier surfaces during polishing, a frequency of dressing of the polishing pads can be reduced, and an

operating rate of the apparatus can be considerably improved. Moreover, since a carrier life is long, a cost can be reduced.

[0042]

Additionally, the carrier 10 for the double-side polishing apparatus according to the present invention can be set between the upper and lower turn tables 12 and 13 having the polishing pads 14 of the double-side polishing apparatus 11 attached thereto, the semiconductor wafer W is held in the holding hole 17 to be sandwiched between the upper and lower turn tables 12 and 13, and the wafer W can be subjected to double-side polishing while supplying the polishing liquid.

[0043]

When such a method is used to carry out double-side polishing, metal contamination can be suppressed, and a wafer having reduced peripheral sag and a high flatness can be stably obtained. Further, since dressing of the polishing pads can be carried out by using the carrier surfaces during polishing, a frequency of dressing of the polishing pads can be reduced, and polishing can be efficiently carried out. Furthermore, since each surface of the carrier made of titanium itself has predetermined roughness, a coating layer of, e.g., abrasive grains can be prevented from being delaminated from each carrier surface to damage the wafer.

[0044]

The present invention will be described in detail below based on examples and comparative examples. However, the present invention is not limited thereto.

(Examples 1 and 2)

A double-side polishing apparatus 11 shown in FIGS. 1 and 2 was prepared. Front and back surfaces of each titanium carrier 10 were roughened by using a diamond pellet in advance. Surface roughness of each carrier surface was measured by using Surf Test SJ-201P manufactured by Mitutoyo, and evaluation was carried out based on JIS B0601-1994. The surface roughness was $Ra=0.28$ to $0.32\ \mu\text{m}$ (Examples 1 and 2). This carrier 10 was used to perform double-side polishing as follows.

[0045]

After performing dressing of polishing pads 14, double-side polishing of each silicon wafer having a diameter of 300 mm was performed. That is, one etched silicon wafer W was set in each of five titanium carriers each having a holding hole 17, an upper turn table 13 was rotated in a clockwise direction whilst a lower turn table 12 was rotated in a counterclockwise direction with a number of revolutions of 20 rpm and a load of $250\ \text{g/cm}^2$, and an alkaline solution containing colloidal silica was used as a polishing liquid. This polishing was repeatedly performed for four times.

[0046]

A peripheral sag amount of each wafer after polishing was measured. Like the above-explained experiment, a wafer shape evaluation apparatus manufactured by Kuroda Precision Industries Ltd. was used to measure a difference in wafer shape between a position that is 1 mm away from a wafer edge and a position that is 3 mm away from the same as a peripheral sag amount with a section from a position that is 30 mm apart from the wafer edge to a position where peripheral sag starts being determined as a reference plane. FIG. 7 shows obtained measurement results.

[0047]

(Comparative Examples 1 and 2)

Double-side polishing and measurement were carried out under the same conditions as those of (Examples 1 and 2) except that each titanium carrier (surface roughness was $R_a=0.02$ to $0.06\ \mu\text{m}$) having non-roughened front and back surfaces was used (Comparative Examples 1 and 2). FIG. 7 shows obtained measurement results.

[0048]

As shown in FIG. 7, it has been confirmed that, when the front and back surfaces of each titanium carrier are roughened to have R_a of $0.14\ \mu\text{m}$ or above, each wafer having reduced peripheral sag and a high flatness can be obtained in each of the four polishing operations.

[0049]

(Examples 3, 4, and 5)

Like Examples 1 and 2, front and back surfaces of each

titanium carrier were roughened by using a diamond pellet ($Ra=0.28$ to $0.32\text{ }\mu\text{m}$), and then grooves having such a grid-like pattern as described in FIG. 6(a) were formed. A groove width was 1 mm , a groove depth was $2\text{ }\mu\text{m}$, and a groove interval was 2 mm . Double-side polishing was performed under the same conditions as those of Examples 1 and 2 except that each carrier having such grooves was used.

[0050]

Further, a peripheral sag amount of each polished wafer was measured like Examples 1 and 2 (Examples 3, 4, and 5).

FIG. 8 shows obtained measurement results.

[0051]

(Examples 6 and 7)

Double-side polishing and measurement were performed under the same conditions as those of (Examples 3, 4, and 5) except that each titanium carrier having no groove formed thereon and $Ra=0.28$ to $0.32\text{ }\mu\text{m}$ was used (Examples 6 and 7). FIG. 8 shows obtained measurement results.

It can be understood from the measurement results of the peripheral sag amount described in FIG. 8 that each wafer according to Examples 3, 4, and 5 has a higher flatness than each wafer according to Examples 6 and 7. In particular, it has been confirmed that the peripheral sag amount according to each of Examples 3, 4, and 5 is far smaller than that according to Examples 6 and 7 and the peripheral sag can be further improved by forming the

grooves on the carrier.

[0052]

(Example 8)

Double-side polishing was performed under the same conditions as those of Examples 1 and 2. Surface roughness of each carrier having front and back surfaces roughened by a diamond pellet was $Ra=0.28$ to $0.32\ \mu\text{m}$.

Observing each polished wafer by using a wafer surface inspection apparatus manufactured by Raytex Corporation, no scratch was observed on each wafer surface (FIG. 9), and it has been confirmed that the high-quality wafer was obtained.

[0053]

(Comparative Example 3)

Each surface of SUS carrier was subjected to blast processing to form an uneven surface having surface roughness $Ra=4.8$ to $5.0\ \mu\text{m}$. Ceramic abrasive grains were deposited on this uneven surface. Double-side polishing was carried out under the same conditions as those of Example 8 except that such carrier was used.

[0054]

Observing each polished wafer by using the wafer surface inspection apparatus manufactured by Raytex Corporation, scratches were observed on the wafer surface (FIG. 9). It can be considered that the abrasive grains deposited on the carrier surfaces fell off to occur scratches on the wafer surface during polishing.

When the carrier having abrasive grains deposited

thereon is used in this manner, a quality of a wafer may be possibly degraded, but using the carrier according to the present invention enables obtaining a high-quality wafer.

[0055]

The present invention is not limited to the embodiment described above. The above-described aspects are mere examples and those having substantially the same structure as technical ideas described in the appended claims and providing the similar functions and advantages are included in the scope of the present invention.

CLAIMS

1. A carrier for double-side polishing apparatus which is set between upper and lower turn tables having polishing pads attached thereto and has a holding hole in which a semiconductor wafer sandwiched between the upper and lower turn tables is held at the time of polishing in a double-side polishing apparatus, wherein a material of the carrier is titanium, and surface roughness of the titanium carrier is $0.14\text{ }\mu\text{m}$ or above in terms of Ra.

2. The carrier for double-side polishing apparatus according to claim 1, wherein the surface roughness is $0.32\text{ }\mu\text{m}$ or above in terms of Ra.

3. The carrier for double-side polishing apparatus according to claim 1 or 2, wherein the carrier has grooves each reaching the holding hole from a carrier outer peripheral side on front and back surfaces thereof.

4. The carrier for double-side polishing apparatus according to claim 3, wherein a pattern of the grooves is a grid-like pattern or a radial pattern.

5. A double-side polishing apparatus comprising at least the carrier for double-side polishing apparatus according to any one of claims 1 to 4.

6. A double-side polishing method for a semiconductor wafer, comprising: arranging the carrier according to any one of claims 1 to 4 between upper and lower turn tables holding the semiconductor wafer in a holding hole formed in the carrier; and sandwiching the semiconductor wafer between the upper and lower turn tables to perform double-side polishing.