Abstract

A semiconductor device has a first conductive layer and a semiconductor die disposed adjacent to the first conductive layer. An encapsulant is deposited over the first conductive layer and semiconductor die. An insulating layer is formed over the encapsulant, semiconductor die, and first conductive layer. A second conductive layer is formed over the insulating layer. A first portion of the first conductive layer is electrically connected to V_{SS} and forms a ground plane. A second portion of the first conductive layer is electrically connected to V_{DD} and forms a power plane. The first conductive layer, insulating layer, and second conductive layer constitute a decoupling capacitor. A microstrip line including a trace of the second conductive layer is formed over the insulating layer and first conductive layer. The first conductive layer is provided on an embedded dummy die, interconnect unit, or modular PCB unit.

(Fig.4)