CLAIMS

1. A system, comprising:

a memory that stores computer executable components; and

a processor, operably coupled to the memory, and that executes the computer executable components stored in the memory, wherein the computer executable components comprise:

an interpolation component that interpolates, using a reference model, a gate parameter for a target stretch factor that has not been calibrated for a quantum gate, wherein the reference model includes reference gate parameters for the quantum gate calibrated at a plurality of reference stretch factors; and

an execution component that executes, via a quantum circuit, a quantum operation using the gate parameter to generate results data, wherein the quantum circuit includes the quantum gate.

2. The system of claim 1, further comprising:

a model component that defines the plurality of reference stretch factors by determining a number of references stretch factors within a stretch factor interval based on at least one of an error per gate determination or a gate parameter determination.

3. The system of claim 2, wherein the number of reference stretch factors included within the stretch factor interval increases with a number of variations in the error per gate determination within the stretch factor interval.

4. The system of claim 2, further comprising:

a mitigation component that generates an error mitigated result by extrapolating the result data to a zero-order noise limit.

5. The system of claim 1, further comprising:

a recommendation component that identifies the target stretch factor based on a gate count and a qubit count of a quantum circuit that includes the quantum gate.

6. A system, comprising:

a memory that stores computer executable components; and

a processor, operably coupled to the memory, and that executes the computer executable components stored in the memory, wherein the computer executable components comprise:

a recommendation component that identifies a stretch factor for error mitigation of a quantum circuit based on a gate count and a qubit count of the quantum circuit; and

an execution component that executes, via the quantum circuit, a quantum operation using a gate parameter, based on the stretch factor, to generate results data.

7. The system of claim 6, wherein the recommendation component compares the gate count and the qubit count of the quantum circuit to a reference table that includes a range of stretch factors associated with defined gate and qubit count combinations.

8. The system of claim 7, further comprising:

a gate resource component that executes a benchmark operation that determines maximum stretch factors associated with a set of quantum gates; and

monitoring component that monitors an availability of one or more quantum gates from the set of quantum gates.

9. The system of claim 8, further comprising:

an adjustment component that adjusts the stretch factor based on at least one of hardware constraints and the maximum stretch factors associated with the one or more quantum gates available for execution of the quantum circuit.

10. The system of claim 9, further comprising:

an interpolation component that interpolates the gate parameter for the adjusted stretch factor from a reference model that includes reference gate parameters for the one or more quantum gates calibrated at a plurality of reference stretch factors.

11. A computer-implemented method, comprising:

interpolating, by a system operatively coupled to a processor, using a reference model, a gate parameter associated with a target stretch factor that has not been calibrated for a quantum gate, wherein the reference model includes reference gate parameters for a quantum gate calibrated at a plurality of reference stretch factors; and

executes, by the system, via a quantum circuit, a quantum operation using the gate parameter to generate results data, wherein the quantum circuit includes the quantum gate.

12. The computer-implemented method of claim 11, further comprising:

determining, by the system, a number of references stretch factors included within a stretch factor interval based on at least one of an error per gate determination or a gate parameter determination.

13. The computer-implemented method of claim 12, wherein the number of reference stretch factors included within the stretch factor interval increases with a number of variations in the error per gate determination within the stretch factor interval, and wherein the number of reference stretch factors included within the stretch factor interval increases with a number of variations in the gate parameter determination within the stretch factor interval.

14. The computer-implemented method of claim 12, further comprising:

generating, by the system, an error mitigated result by extrapolating the result data to a zero-order noise limit.

15. The computer-implemented method of claim 14, further comprising:

identifying, by the system, the target stretch factor based on a gate count and a qubit count of a quantum circuit that includes the quantum gate.

16. A computer-implemented method, comprising:

recommending, by a system operatively coupled to a processor, a stretch factor for error mitigation of a quantum circuit based on a gate count and a qubit count of the quantum circuit; and

executing, by the system, via the quantum circuit, a quantum operation using a gate parameter, based on the stretch factor, to generate results data.

17. The computer-implemented method of claim 16, wherein the recommending compares the gate count and the qubit count of the quantum circuit to a reference table that includes a range of stretch factors associated with defined gate and qubit count combinations.

18. The computer-implemented method of claim 16, further comprising:

executing, by the system, a benchmark operation that determines maximum stretch factors associated with a set of quantum gates; and

monitoring, by the system, an availability of one or more quantum gates from the set of quantum gates.

19. The computer-implemented method of claim 16, further comprising:

adjusting, by the system, the stretch factor based on and least one of the hardware constraints and the maximum stretch factors associated with the one or more quantum gates available for execution of the quantum circuit.

20. The computer-implemented method of claim 19, further comprising:

interpolating, by the system, the gate parameter for the adjusted stretch factor from a reference model that includes reference gate parameters for the one or more quantum gates calibrated at a plurality of reference stretch factors.

21. A computer program product for quantum computer error mitigation, the computer program product comprising a computer readable storage medium having program instructions embodied therewith, the program instructions executable by a processor to cause the processor to:

interpolate, by the processor, using a reference model, a gate parameter associated with a target stretch factor that has not been calibrated for a quantum gate, wherein the reference model includes reference gate parameters for the quantum gate calibrated at a plurality of reference stretch factors; and

execute, by the processor, via a quantum circuit, a quantum operation using the gate parameter to generate results data, wherein the quantum circuit includes the quantum gate.

22. The computer program product of claim 21, wherein the program instructions further cause the processor to:

define, by the processor, the plurality of reference stretch factors by determining a number of references stretch factors within a stretch factor interval based on at least one of an error per gate determination or a gate parameter determination.

23. The computer program product of claim 21, wherein the program instructions further cause the processor to:

identify, by the processor, a recommended stretch factor from the range of stretch factors based on a gate count and a qubit count of a quantum circuit that includes the quantum gate.

24. The computer program product of claim 23, wherein the program instructions further cause the processor to:

compare, by the processor, the gate count and the qubit count of the quantum circuit to a reference table that includes a range of stretch factors associated with defined gate and qubit count combinations.

25. The computer program product of claim 24, wherein the program instructions further cause the processor to:

generate, by the processor, result data by executing a quantum operation on a quantum circuit that includes the quantum gate using the gate parameter; and

generate, by the processor, an error mitigated result by extrapolating the result data to a zero-order noise limit.