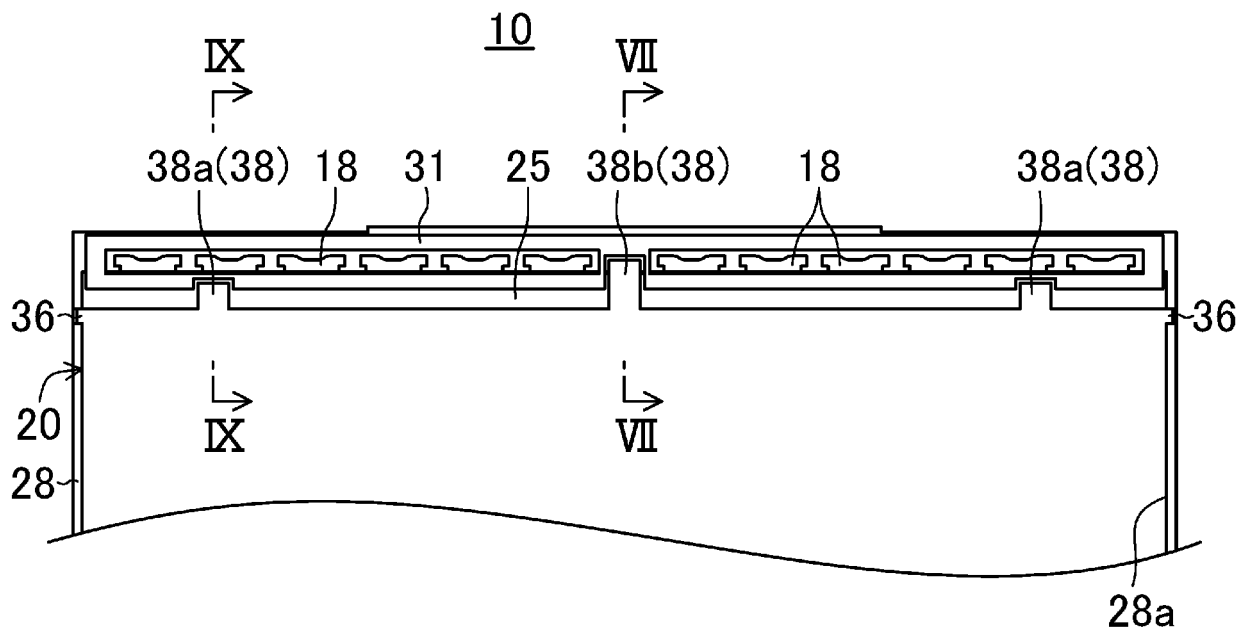
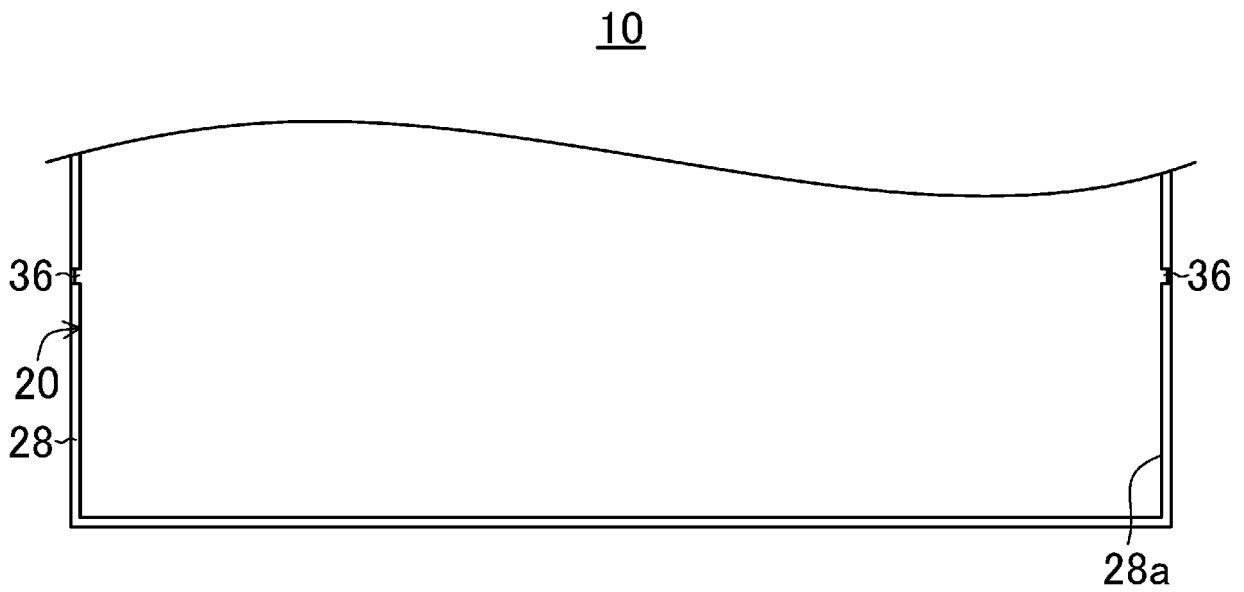


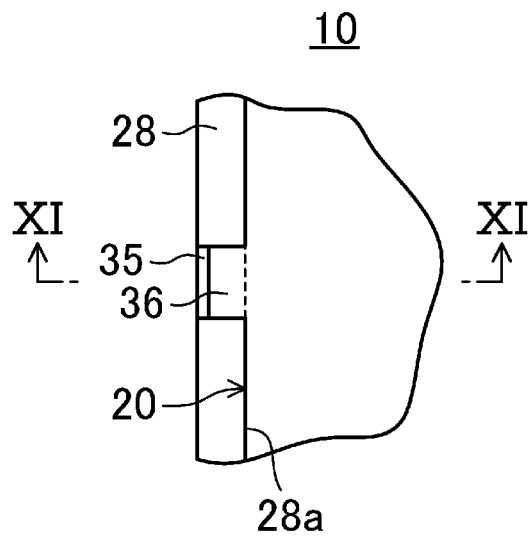
[図1]



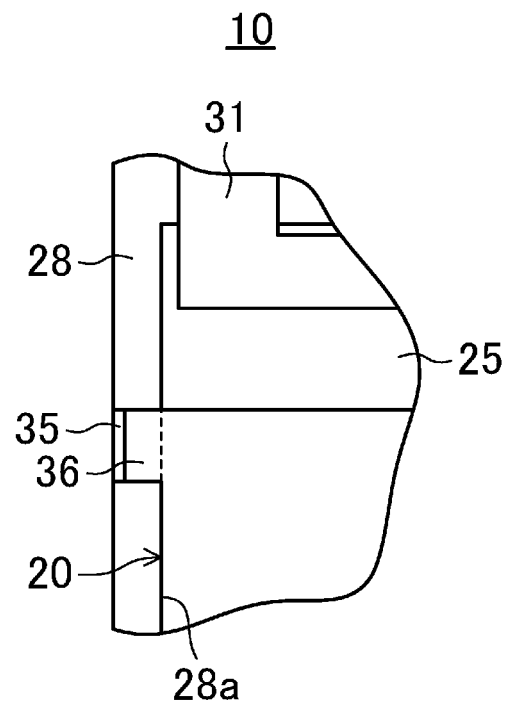
[図2]



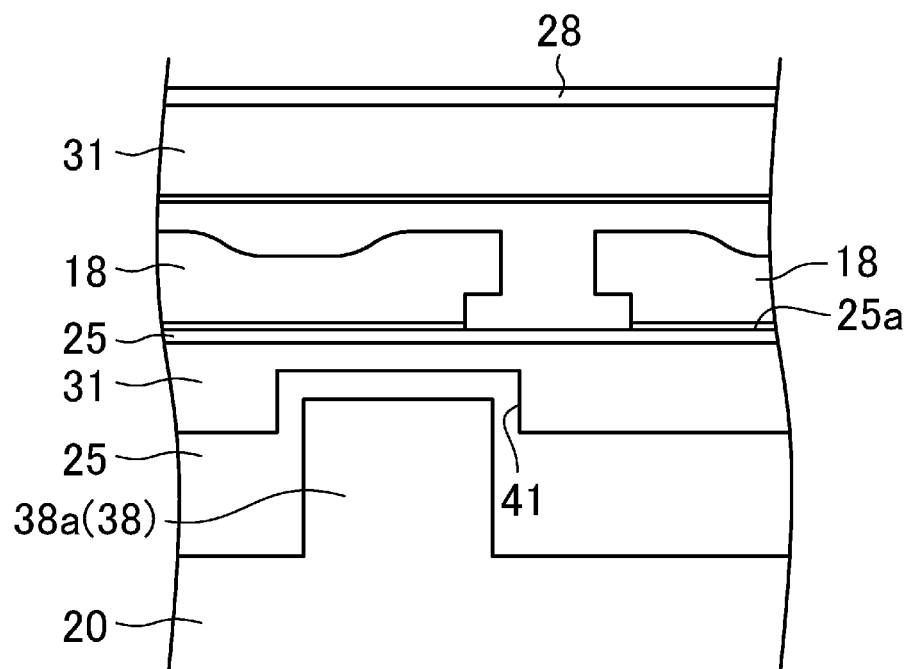
[図3]



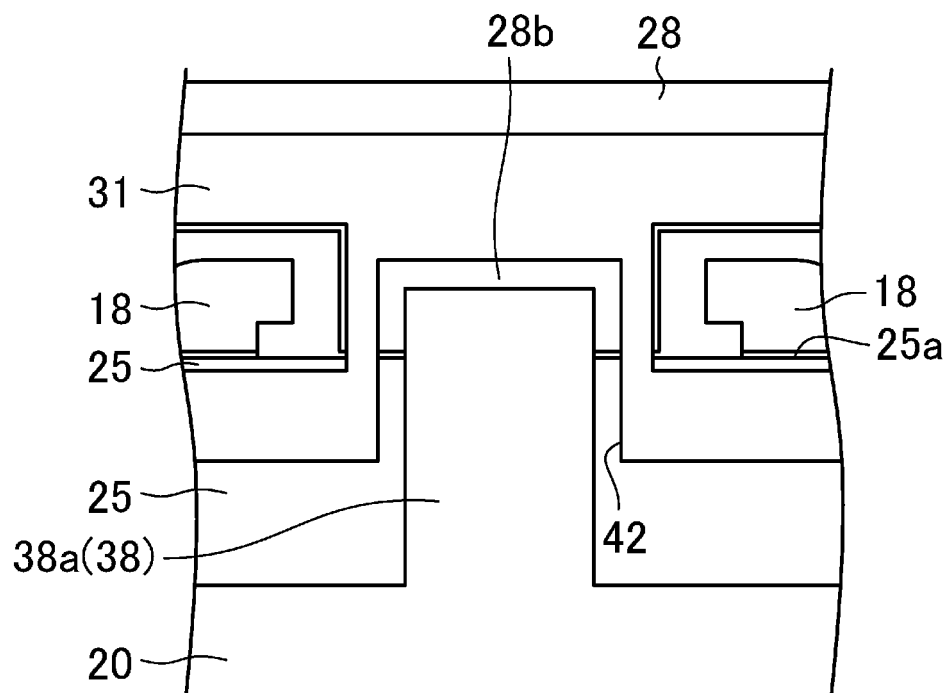
[図4]



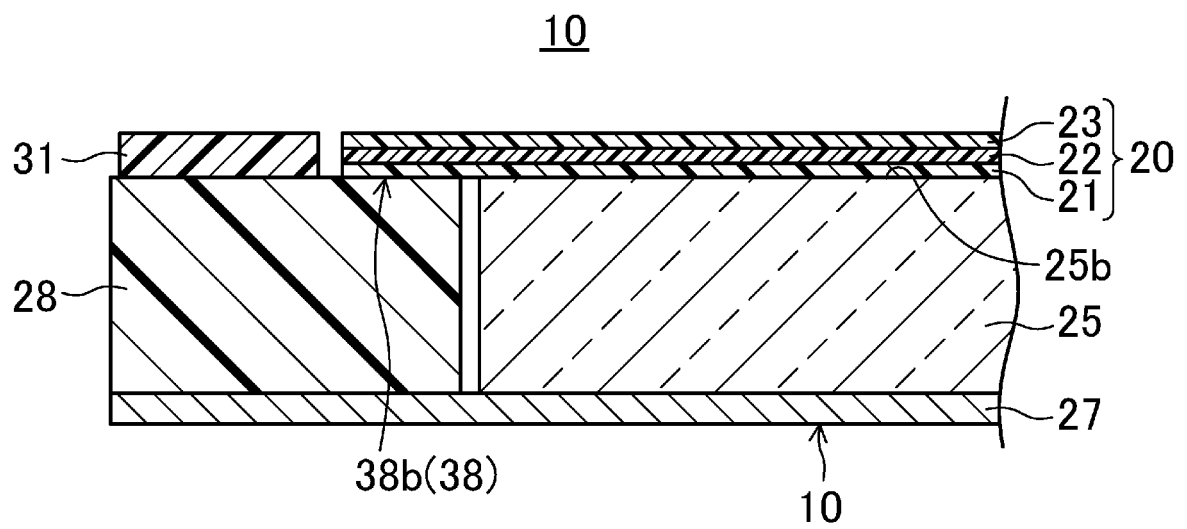
[図5]



[図6]



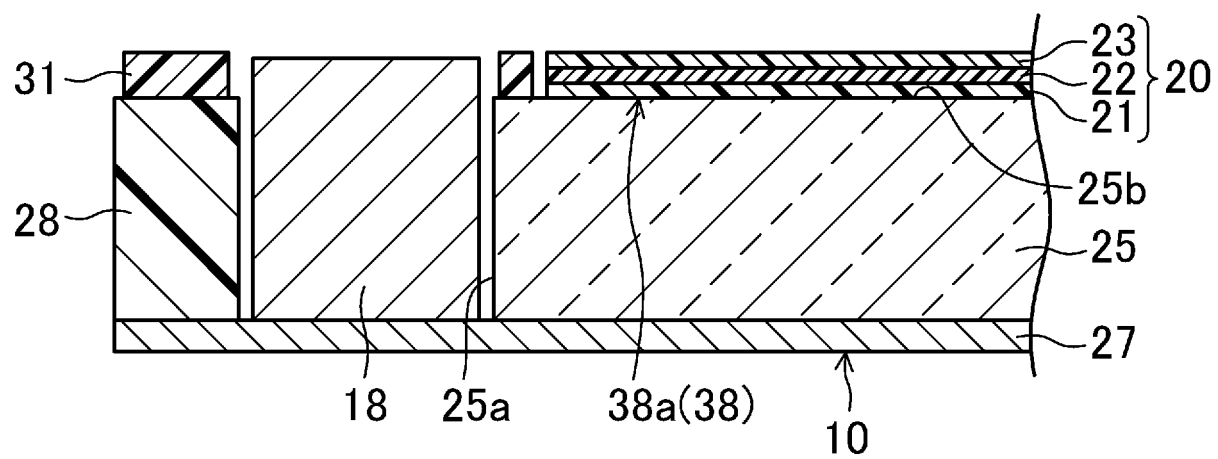
[図7]



1



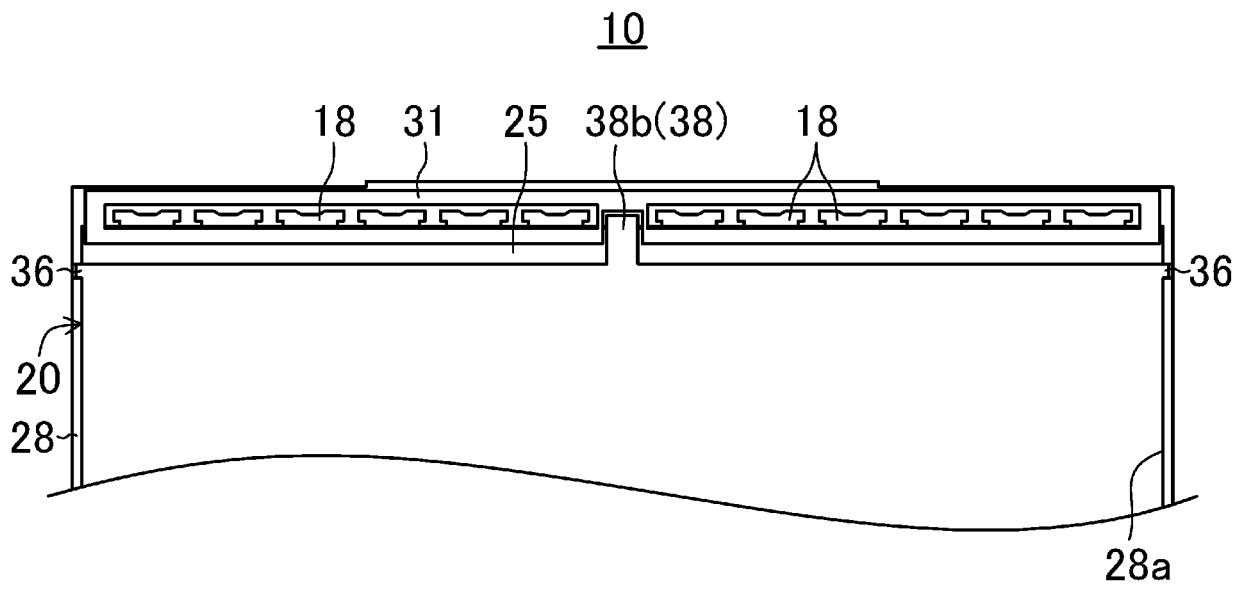
10



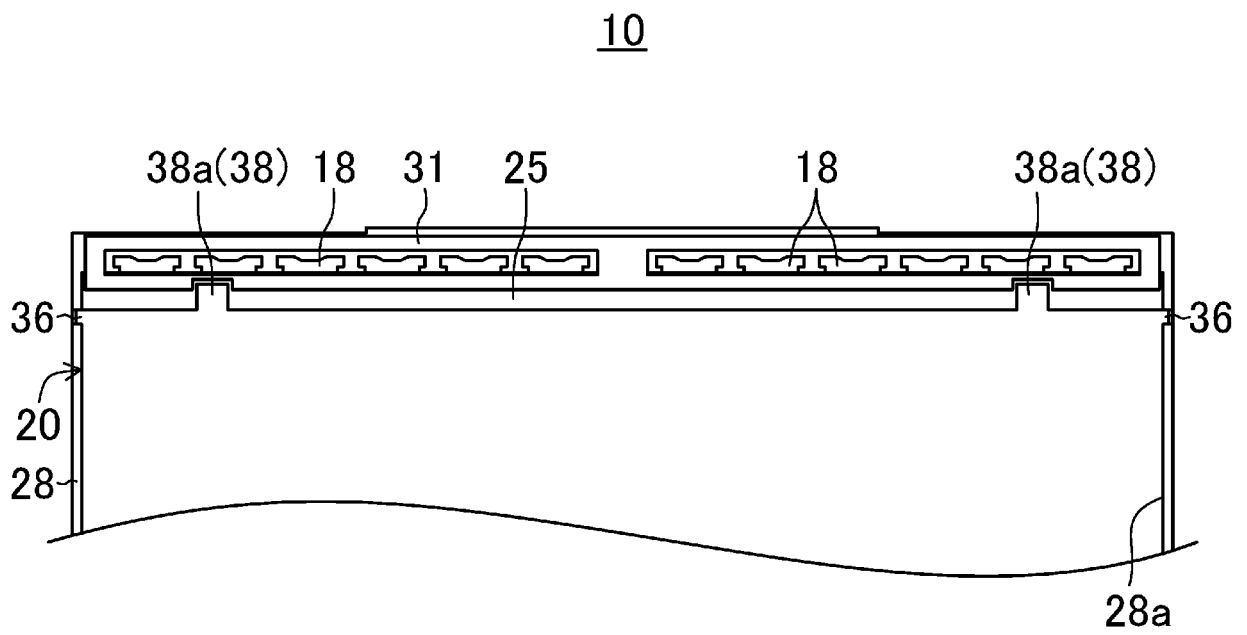
A detailed cross-sectional view of a semiconductor device 1. The device features a substrate 10 with a base layer 27. A central region 25 contains a core 25a and is surrounded by a material 25b. A layer 21 is positioned above the core 25a, with a sub-layer 22. A patterned layer 23 is on top of layer 21. A thick layer 11 covers the top, with a thin layer 12 on its surface. A layer 13 is located between the thick layer 11 and the patterned layer 23. A layer 14 is on the right side. A layer 15 is on the top right. A layer 16 is on the top left. A layer 17 is on the top left. A layer 18 is on the bottom left. A layer 28 is on the bottom left. A layer 30 is on the bottom left. A layer 31 is on the bottom left. A layer 32 is on the bottom left. A layer 38a(38) is on the bottom right. A layer 20 is on the right side, encompassing layers 21, 22, and 23.

A detailed cross-sectional view of a semiconductor device 10. The device features a substrate 25 with a base layer 27. A central region 25b is defined by a vertical wall 36. A series of layers are stacked on top of the substrate, including a layer 21, a layer 22, and a layer 23, which are collectively labeled as 20. A layer 13 is positioned above layer 23. A layer 11 is positioned above layer 13. A layer 12 is positioned above layer 11. A layer 14 is positioned above layer 12. A layer 15 is positioned above layer 14. A layer 33 is positioned above layer 15. A layer 35 is positioned above layer 33. A layer 28 is positioned above layer 35. A layer 36 is positioned above layer 28. A layer 10 is positioned above layer 36. A layer 27 is positioned above layer 10.

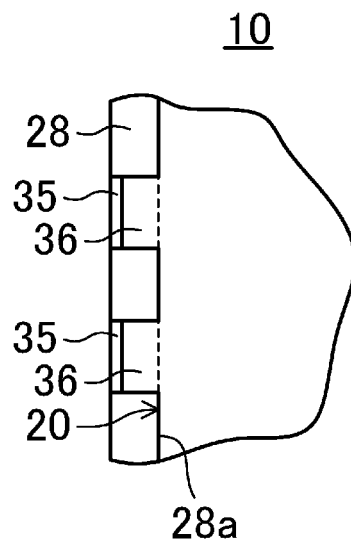
[図12]



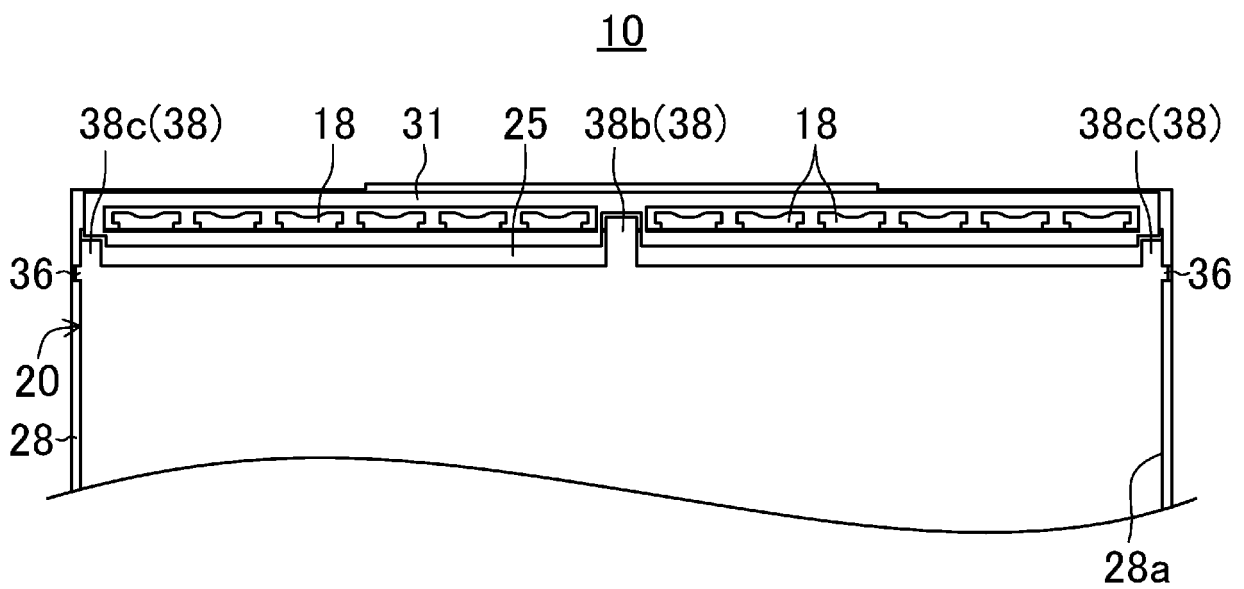
[図13]



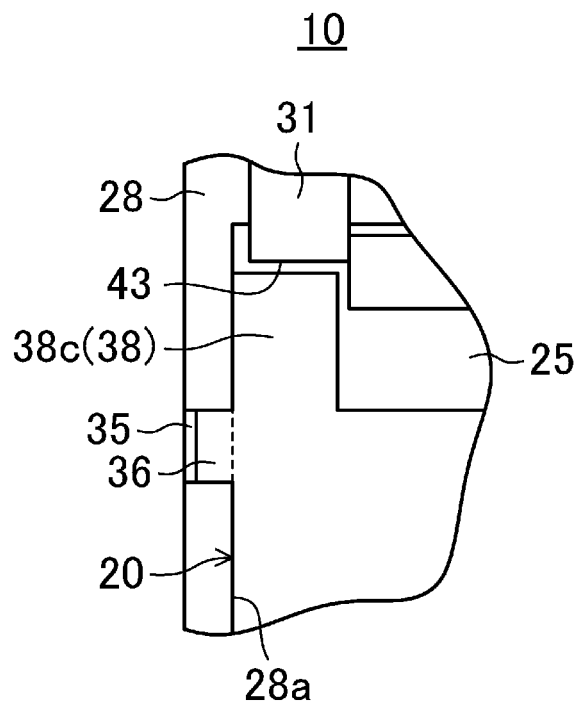
[図14]



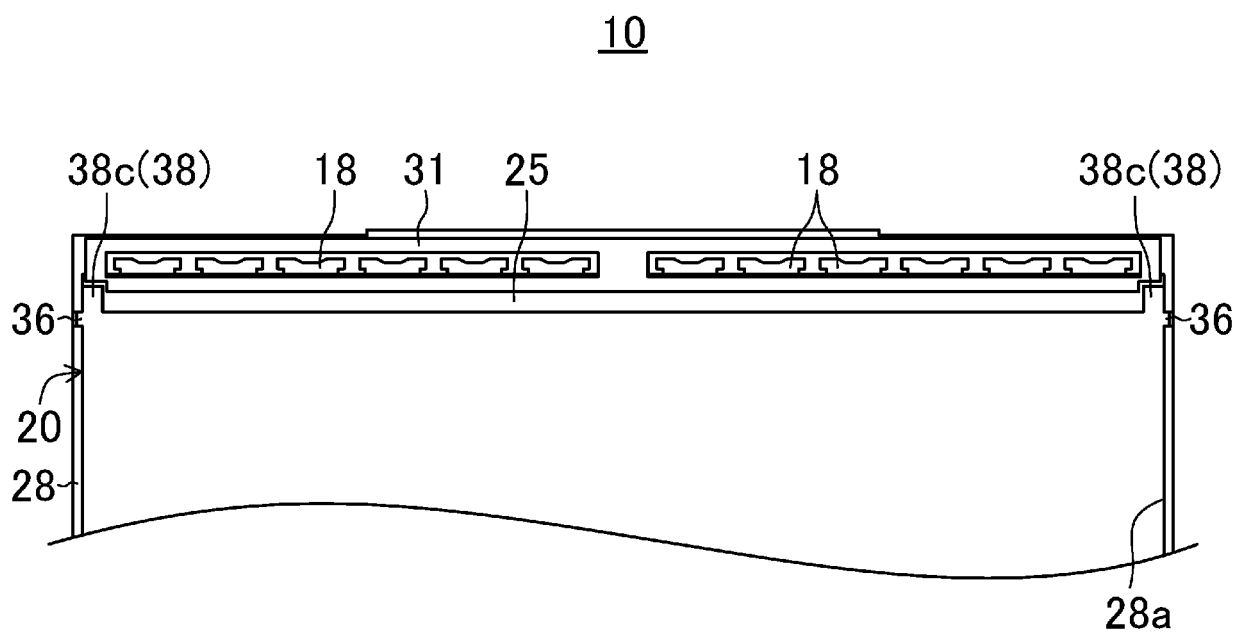
[図15]



[図16]



[図17]



[図18]

