

Claims

1. A wafer geometry measurement method comprising: obtaining geometry measurements of a three-dimensional NAND structure utilizing a wafer geometry measurement tool; and applying, with one or more processors, a multi-layer stack correction model to correct the geometry measurements obtained by the wafer geometry measurement tool from the three-dimensional NAND structure, wherein the multi-layer stack correction model includes a simulated correction curve representing a correlation between a true thickness and a measured thickness, wherein the multi-layer stack correction model is configured to correct one or more measurement errors in topographical data caused by a transparent film positioned on the three-dimensional NAND structure based on reflectivity and phase change information measured from the transparent film; and providing one or more control signals to one or more process tools in a semiconductor fabrication facility based on the corrected geometry measurements.
2. The method of claim 1, wherein the correction model is obtained at least partially based on correlations between true wafer thickness data and wafer thickness data measured using the wafer geometry measurement tool.
3. The method of claim 1, wherein the correction model is obtained at least partially based on a design of the wafer and known physical and optical properties of a plurality of layers of the wafer.
4. The method of claim 1, wherein the correction model further takes into account a wafer map with reflectivity information.
5. The method of claim 4, wherein the wafer map with reflectivity information is obtained utilizing a single wavelength interferometer that collects spatial information from multiple wafer surface locations.
6. The method of claim 1, wherein the correction curve supports wrapping and unwrapping.
7. A wafer geometry measurement method comprising: generating a multi-layer stack correction model at least partially based on a design of a wafer and known physical and optical properties of a three-dimensional NAND structure of the wafer, wherein the multi-layer stack correction model includes a simulated correction curve representing a correlation between a true thickness and a measured thickness; obtaining geometry measurements of the wafer utilizing a wafer geometry measurement tool; applying the correction model to correct the geometry measurements obtained by the wafer geometry measurement tool, wherein the correction model is configured to correct measurement errors in topographical data caused by a transparent film positioned on the three-dimensional NAND structure of the wafer; and providing one or more control signals to one or more process tools in a semiconductor fabrication facility based on the corrected geometry measurements.

8. The method of claim 7, wherein the correction model is generated at least partially based on correlations between true wafer thickness data and wafer thickness data measured using the wafer geometry measurement tool.
9. The method of claim 7, wherein the correction model further takes into account for a wafer map with reflectivity information.
10. The method of claim 9, wherein the wafer map with reflectivity information is obtained utilizing a single wavelength interferometer that collects spatial information from multiple wafer surface locations.
11. The method of claim 7, wherein the correction curve supports wrapping and unwrapping.
12. A system comprising: one or more wafer geometry measurement tools configured to obtain geometry measurements of a three-dimensional NAND structure of a wafer; and one or more processors in communication with the one or more wafer geometry measurement tools, the one or more processors configured to: apply a multi-layer stack correction model to correct the geometry measurements obtained by the wafer geometry measurement tool from the three-dimensional NAND structure, wherein the multi-layer stack correction model includes a simulated correction curve representing a correlation between a true thickness and a measured thickness, wherein the multi-layer stack correction model is configured to correct one or more measurement errors in topographical data caused by a transparent film positioned on the three-dimensional NAND structure based on reflectivity and phase change information measured from the transparent film; and provide one or more control signals to one or more process tools in a semiconductor fabrication facility based on the corrected geometry measurements.
13. The system of claim 12, wherein the correction model is obtained at least partially based on correlations between true wafer thickness data and wafer thickness data measured using the wafer geometry measurement tool.
14. The system of claim 12, wherein the correction model is obtained at least partially based on a design of the wafer and known physical and optical properties of a plurality of layers of the wafer.
15. The system of claim 12, wherein the correction model further takes into account for a wafer map with reflectivity information.
16. The system of claim 15, wherein the wafer map with reflectivity information is obtained utilizing a single wavelength interferometer that collects spatial information from multiple wafer surface locations.
17. The method of claim 12, wherein the correction curve supports wrapping and unwrapping.