CLAIMS

1. ~~A~~ structure comprising:

~~an~~ array of memory cells, a memory cell comprises~~:~~

~~at least one~~ a plurality of metal-oxide-semiconductor (MOS) elements, the plurality of MOS elements comprising:

a first MOS element, wherein a source terminal of the ~~at least one~~first MOS element is connected to a drain terminal of the first MOS element, and the source terminal ~~being connected to~~ and the drain terminal ~~causes~~of the ~~at least one~~first MOS element is connected to a first bias;

a second MOS element, wherein a source terminal of the second MOS element is connected to a drain terminal of the second MOS element, and the source terminal and the drain terminal of the second MOS element is connected to the first bias;

a third MOS element, wherein a source terminal of the third MOS element is connected to a drain terminal of the third MOS element, and the source terminal and the drain terminal of the third MOS element is connected to a second bias;

a fourth MOS element, wherein a source terminal of the fourth MOS element is connected to a drain terminal of the fourth MOS element, and the source terminal and the drain terminal of the fourth MOS element is connected to the second bias;

wherein the connections between the source terminals and the drain terminals of the first MOS element, the second MOS element, the third MOS element, and the fourth MOS element causes the plurality of MOS elements to exhibit capacitive behavior for storing electrical energy;

a first transistor connected to the ~~at least one~~plurality of MOS ~~element~~elements, wherein activation of the first transistor facilitates a write operation to the memory cell; ~~and~~

a second transistor connected to the ~~at least one~~plurality of MOS ~~element~~elements, wherein activation of the second transistor facilitates a read operation from the memory cell~~.~~; and

a plurality of analog circuits configured to accumulate and store electrical energy outputted from a corresponding column of memory cells among the array of memory cells, each analog circuit among the plurality of analog circuits comprises an input transistor driven by the electrical energy outputted from the corresponding column of memory cells, wherein the input transistor is connected in series with a p-channel metal-oxide-semiconductor (PMOS) switch and a n-channel metal-oxide-semiconductor (NMOS) switch, and a gate of the PMOS switch and a gate of the NMOS switch are driven by a pair of complementary signals.

2. The structure of claim 1, wherein the electrical energy being stored in a column of the memory cells is accumulated to represent a weight in an artificial neural network.

3. The structure of claim 1, wherein the ~~at least one~~first MOS element ~~comprises~~is a first p-channel metal-oxide-semiconductor (PMOS) transistor, the second MOS element is a second PMOS transistor, the third MOS element is a first n-channel metal-oxide-semiconductor (NMOS ~~transistor,~~), and the fourth MOS element a second NMOS transistor.

4. The structure of claim 3, wherein the first PMOS transistor and the second PMOS transistor are connected in parallel, the first NMOS transistor and the second NMOS transistor are connected in parallel.

5. The structure of claim 1, wherein:

the first transistor is a first NMOS transistor;

the second transistor is a second NMOS transistor;

a drain terminal of the first NMOS transistor is connected to a bit line true (BLT) wire;

a source terminal of the first NMOS transistor is connected to the ~~at least one~~plurality of MOS ~~element~~elements;

a drain terminal of the second NMOS transistor is connected to the ~~at least one~~plurality of MOS ~~element~~elements; and

a source terminal of the second NMOS transistor is connected to a bit line complimentary (BLC) wire.

6. The structure of claim 5, wherein:

a gate of the first NMOS transistor is controlled by a first clock signal;

a gate of the second NMOS transistor is controlled by a second clock signal;

in response to the first clock signal activating the first NMOS transistor, an input from the BLT wire is transmitted to the ~~at least one~~plurality of MOS ~~element~~elements; and

in response to the second clock signal activating the second NMOS, a voltage difference between the BLT wire and the BLC wire is outputted.

7. The structure of claim 1, further comprising at least one circuit configured to bias the capacitance of the ~~at least one~~plurality of MOS ~~element~~elements.

8. The structure of claim 1, wherein the array of memory cells is integrated with a non-volatile memory.

~~9. The structure of claim 1, further comprising a plurality of analog circuits configured to accumulate and store electrical energy outputted from a corresponding column of memory cells.~~

~~10.~~

9. A system comprising:

a memory;

a processor configured to be in communication with the memory;

a structure ~~as claimed in any preceding claim,~~ configured to be in communication with the memory and the processor~~.~~, the structure comprises:

~~11. A memory device comprising:~~

~~an~~ an array of memory cells, a memory cell comprises a plurality of metal-oxide-semiconductor (MOS) elements, the plurality of MOS elements comprises:

a first MOS element, wherein a source terminal of the first MOS element is connected to a drain terminal of the first MOS element, and the source terminal and the drain terminal of the first MOS element is connected to a first bias;

a second MOS element, wherein a source terminal of the second MOS element is connected to a drain terminal of the second MOS element, and the source terminal and the drain terminal of the second MOS element is connected to the first bias;

a third MOS element, wherein a source terminal of the third MOS element is connected to a drain terminal of the third MOS element, and the source terminal and the drain terminal of the third MOS element is connected to a second bias;

a fourth MOS element, wherein a source terminal of the fourth MOS element is connected to a drain terminal of the fourth MOS element, and the source terminal and the drain terminal of the fourth MOS element is connected to the second bias;

wherein the connections between the source terminals and the drain terminals of the first MOS element, the second MOS element, the third MOS element, and the fourth MOS element causes the plurality of MOS elements to exhibit capacitive behavior for storing electrical energy;

a first transistor connected to the plurality of MOS elements, wherein activation of the first transistor facilitates a write operation to the memory cell;

a second transistor connected to the plurality of MOS elements, wherein activation of the second transistor facilitates a read operation from the memory cell;

a plurality of analog circuits configured to accumulate and store electrical energy outputted from a corresponding column of memory cells among the array of memory cells, each analog circuit among the plurality of analog circuits comprises an input transistor driven by the electrical energy outputted from the corresponding column of memory cells, wherein the input transistor is connected in series with a PMOS switch and a NMOS switch, and a gate of the PMOS switch and a gate of the NMOS switch are driven by a pair of complementary signals; and

the processor being configured to generate one or more control signals to control the write and read operations of the array of memory cells.

10. The system of claim 9, wherein the electrical energy being stored in a column of the memory cells is accumulated to represent a weight in an artificial neural network.

11. The system of claim 9, wherein the first MOS element is a first p-channel metal-oxide-semiconductor (PMOS) transistor, the second MOS element is a second PMOS transistor, the third MOS element is a first n-channel metal-oxide-semiconductor (NMOS), and the fourth MOS element a second NMOS transistor.

12. The system of claim 11, wherein the first PMOS transistor and the second PMOS transistor are connected in parallel, the first NMOS transistor and the second NMOS transistor are connected in parallel.

13. The system of claim 9, wherein:

the first transistor is a first NMOS transistor;

the second transistor is a second NMOS transistor;

a drain terminal of the first NMOS transistor is connected to a bit line true (BLT) wire;

a source terminal of the first NMOS transistor is connected to the plurality of MOS elements;

a drain terminal of the second NMOS transistor is connected to the plurality of MOS elements; and

a source terminal of the second NMOS transistor is connected to a bit line complimentary (BLC) wire.

14. The system of claim 9, wherein:

a gate of the first NMOS transistor is controlled by a first clock signal;

a gate of the second NMOS transistor is controlled by a second clock signal;

in response to the first clock signal activating the first NMOS transistor, an input from the BLT wire is transmitted to the plurality of MOS elements; and

in response to the second clock signal activating the second NMOS, a voltage difference between the BLT wire and the BLC wire is outputted.

15. The system of claim 9, wherein the structure further comprises at least one circuit configured to bias the capacitance of the plurality of MOS elements.

16. The system of claim 9, wherein the memory is a non-volatile memory, and the structure is integrated with the memory.

17. A memory device comprising:

a non-volatile memory configured to store data; ~~and,~~

~~a~~ a structure ~~as claimed in any of claims 1 to 9~~ coupled to the non-volatile memory ~~.~~, the structure comprises an array of memory cells, a memory cell comprises a plurality of metal-oxide-semiconductor (MOS) elements, the plurality of MOS elements comprising:

a first MOS element, wherein a source terminal of the first MOS element is connected to a drain terminal of the first MOS element, and the source terminal and the drain terminal of the first MOS element is connected to a first bias;

a second MOS element, wherein a source terminal of the second MOS element is connected to a drain terminal of the second MOS element, and the source terminal and the drain terminal of the second MOS element is connected to the first bias;

a third MOS element, wherein a source terminal of the third MOS element is connected to a drain terminal of the third MOS element, and the source terminal and the drain terminal of the third MOS element is connected to a second bias;

a fourth MOS element, wherein a source terminal of the fourth MOS element is connected to a drain terminal of the fourth MOS element, and the source terminal and the drain terminal of the fourth MOS element is connected to the second bias;

wherein the connections between the source terminals and the drain terminals of the first MOS element, the second MOS element, the third MOS element, and the fourth MOS element causes the plurality of MOS elements to exhibit capacitive behavior for storing electrical energy;

a first transistor connected to the plurality of MOS elements, wherein activation of the first transistor facilitates a write operation to the memory cell;

a second transistor connected to the plurality of MOS elements, wherein activation of the second transistor facilitates a read operation from the memory cell; and

wherein the write operation changes the capacitance of the plurality of MOS elements, and the changed capacitance updates the data stored in the non-volatile memory; and

a plurality of analog circuits configured to accumulate and store electrical energy outputted from a corresponding column of memory cells among the array of memory cells, each analog circuit among the plurality of analog circuits comprises an input transistor driven by the electrical energy outputted from the corresponding column of memory cells, wherein the input transistor is connected in series with a PMOS switch and a NMOS switch, and a gate of the PMOS switch and a gate of the NMOS switch are driven by a pair of complementary signals.

18. The memory device of claim 17, wherein the read operation facilitates a read out of the data stored in the non-volatile memory as a voltage.