FIG. 1

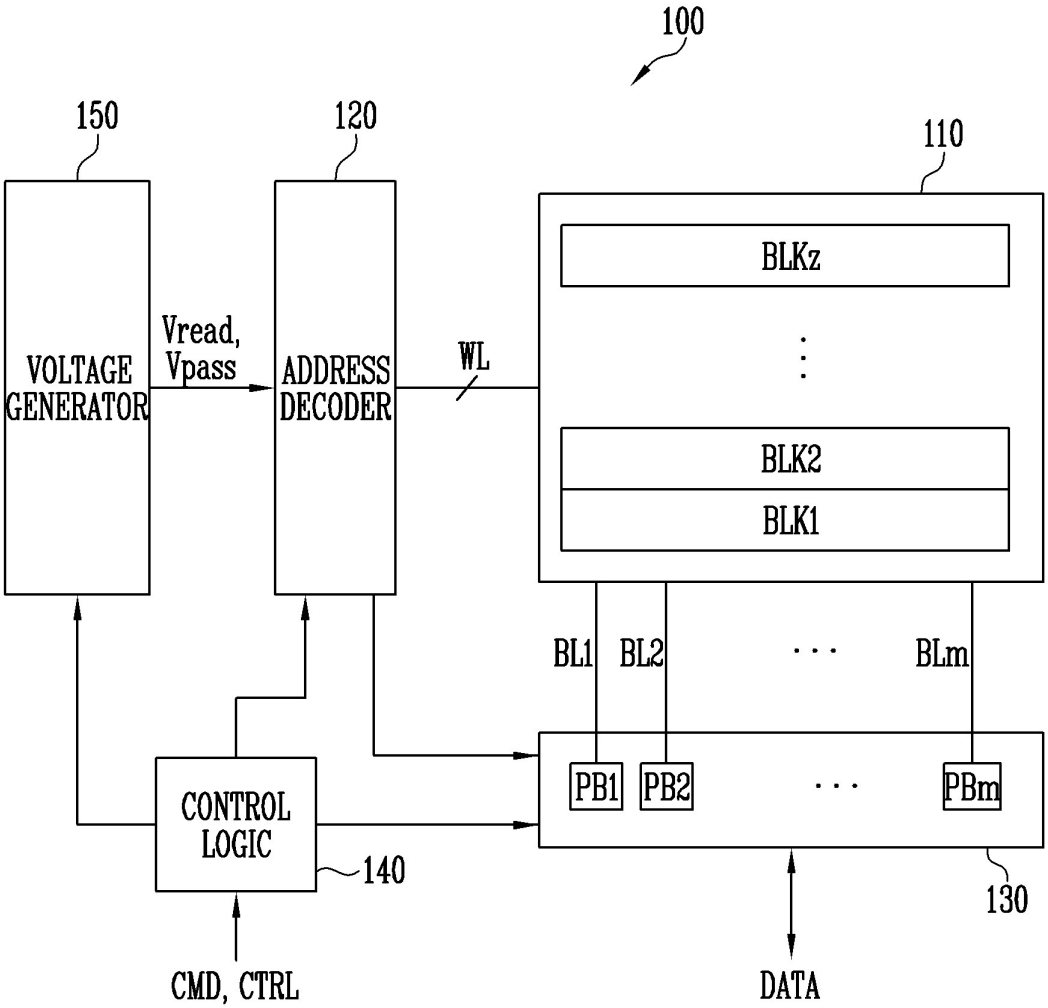

100
150
120
110
VOLTAGE GENERATOR
Vread, Vpass
ADDRESS DECODER
WL
BLKz
BLK2
BLK1
BL1
BL2
BLm
PB1
PB2
PBm
CONTROL LOGIC
140
130
CMD, CTRL
DATA

FIG. 2

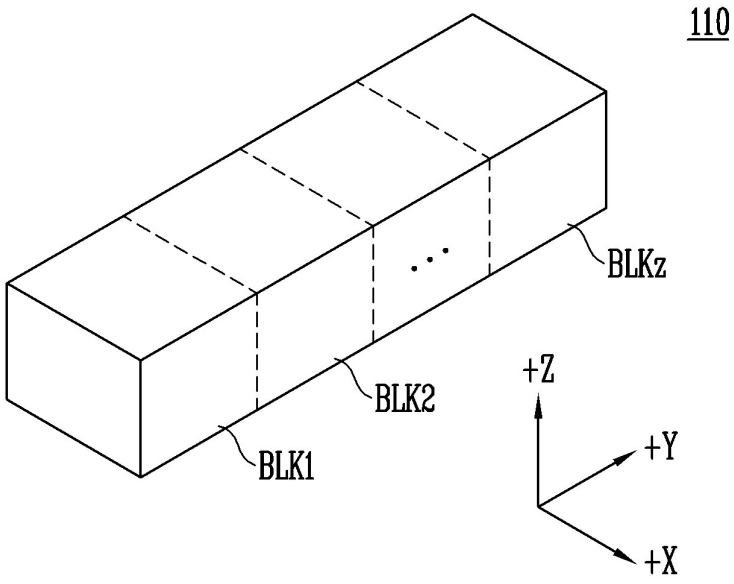


FIG. 3

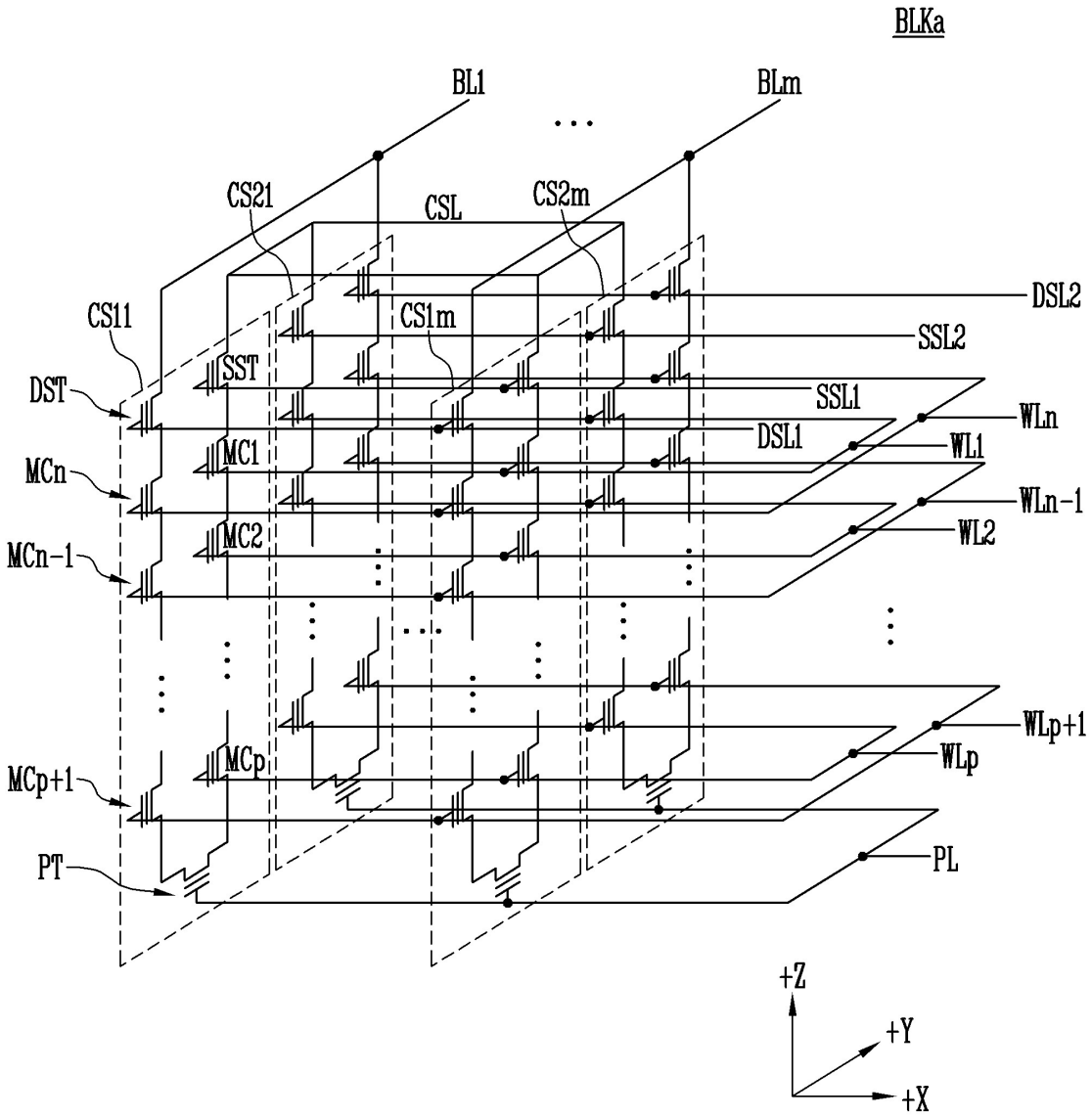

BLKa
BL1
BLm
CS21
CSL
CS2m
CS11
CS1m
DSL2
SSL2
SST
DST
SSL1
WLn
DSL1
WL1
MCn
MC1
WLn-1
MC2
WL2
MCn-1
WLp+1
MCp
WLp
MCp+1
PT
PL
+Z
+Y
+X

FIG. 4

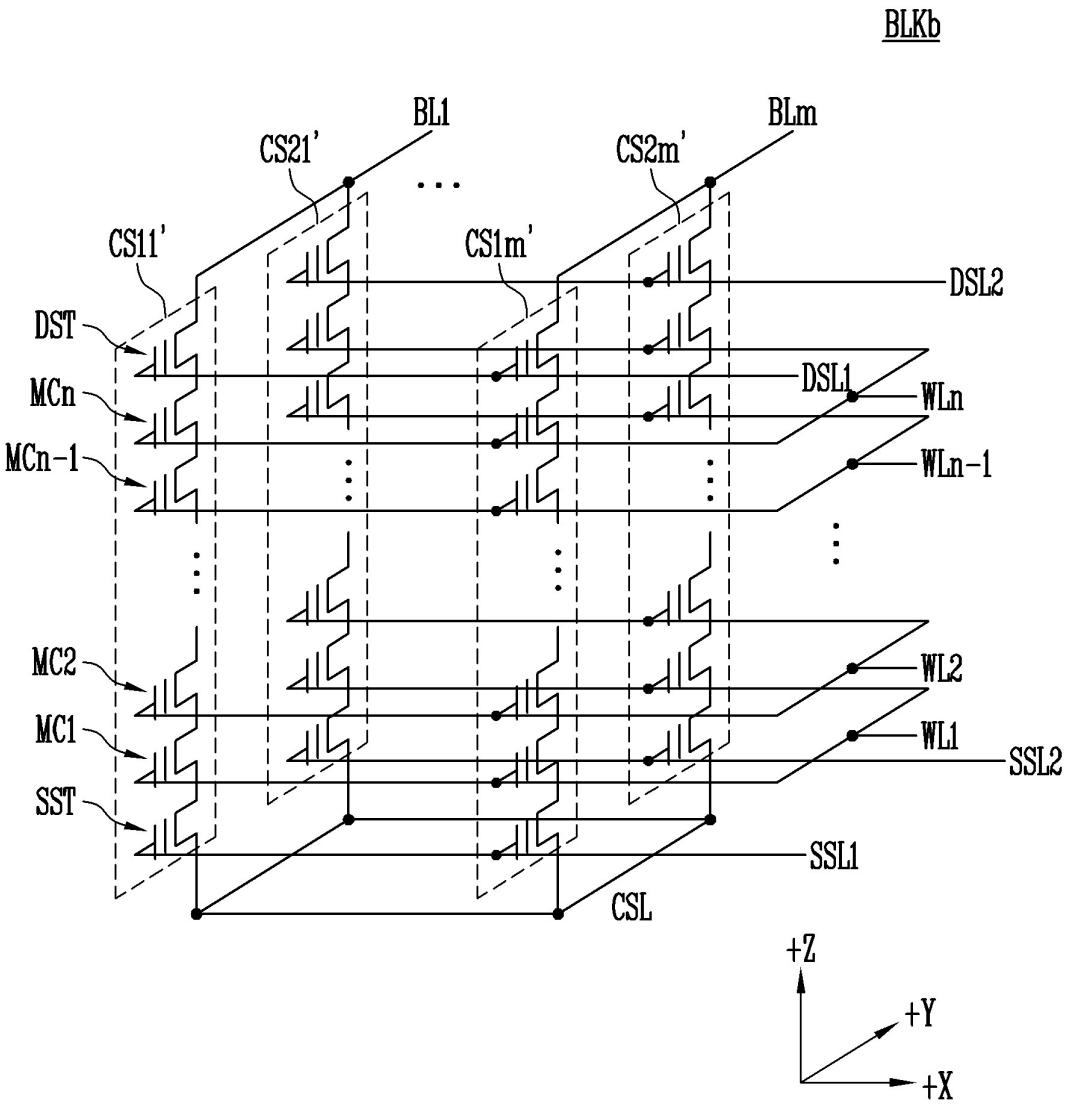

BLKb
BL1
BLm
CS21'
CS2m'
CS11'
CS1m'
DSL2
DST
DSL1
MCn
WLn
MCn-1
WLn-1
MC2
WL2
MC1
WL1
SSL2
SST
SSL1
CSL
+Z
+Y
+X

FIG. 5

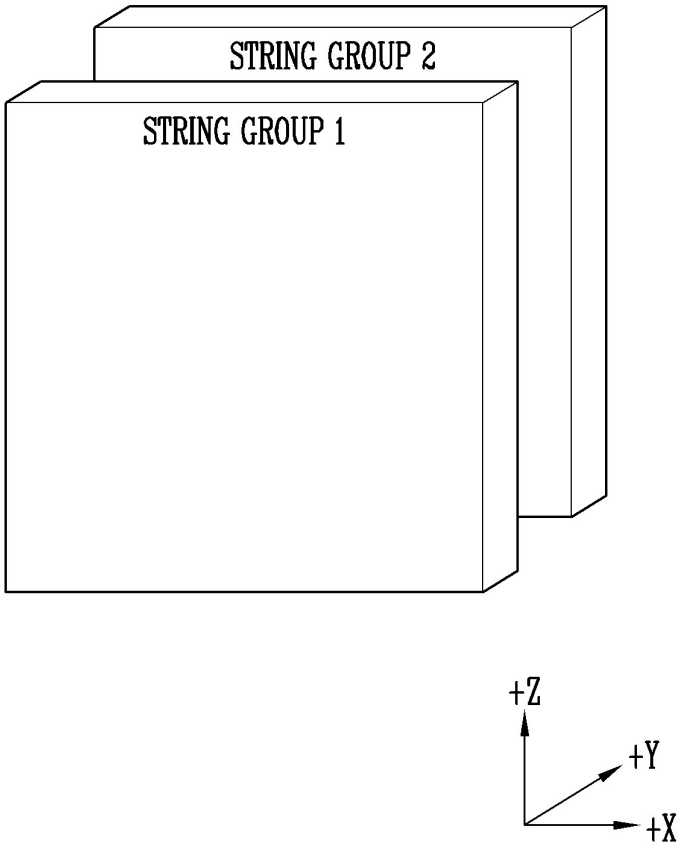


FIG. 6A

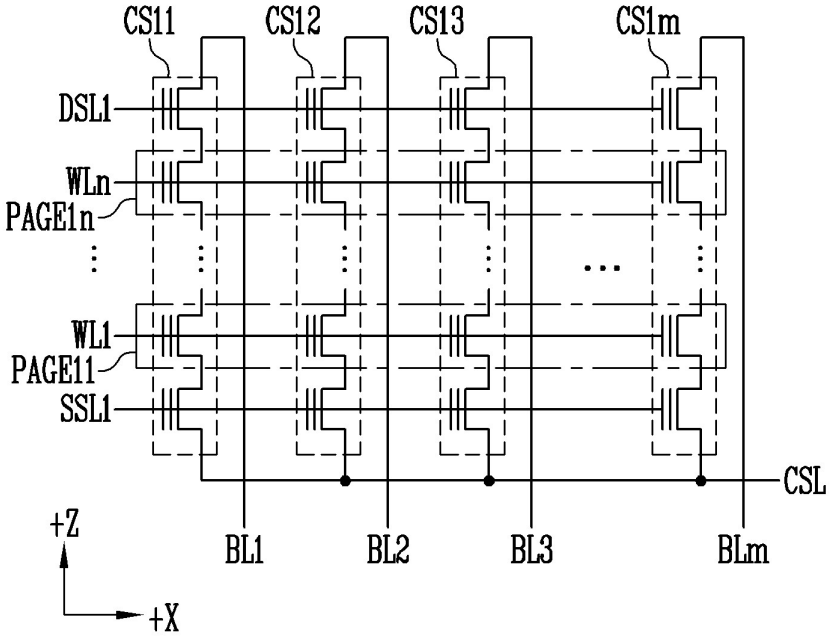

CS11
CS12
CS13
CS1m
DSL1
WLn
PAGE1n
WL1
PAGE11
SSL1
CSL
BL1
BL2
BL3
BLm
+Z
+X

FIG. 6B

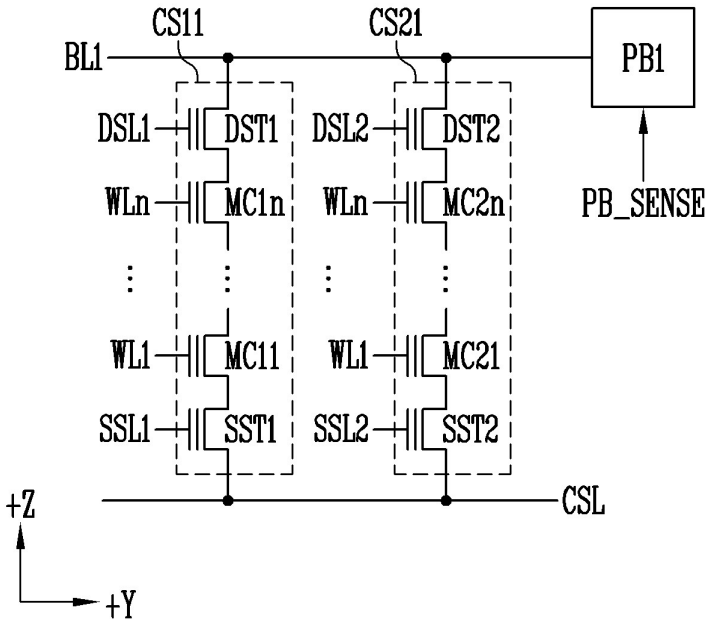

CS11
CS21
BL1
PB1
DSL1
DST1
DSL2
DST2
WLn
MC1n
WLn
MC2n
PB_SENSE
WL1
MC11
WL1
MC21
SSL1
SST1
SSL2
SST2
CSL
+Z
+Y

FIG. 7

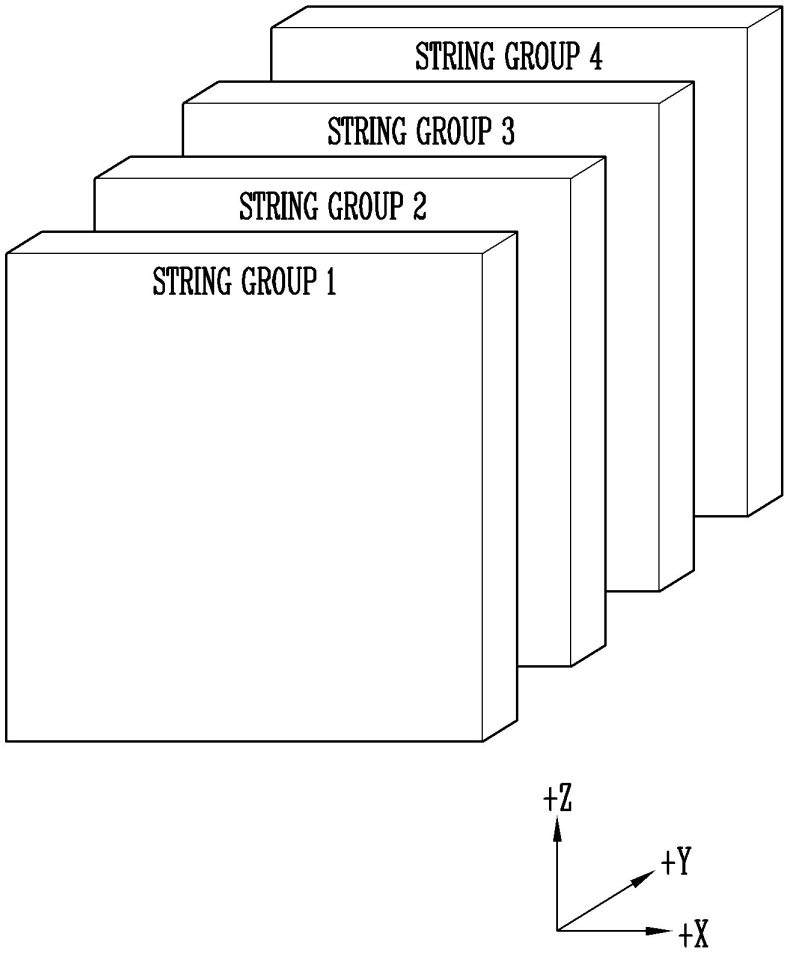

STRING GROUP 4
STRING GROUP 3
STRING GROUP 2
STRING GROUP 1
+Z
+Y
+X

FIG. 8A

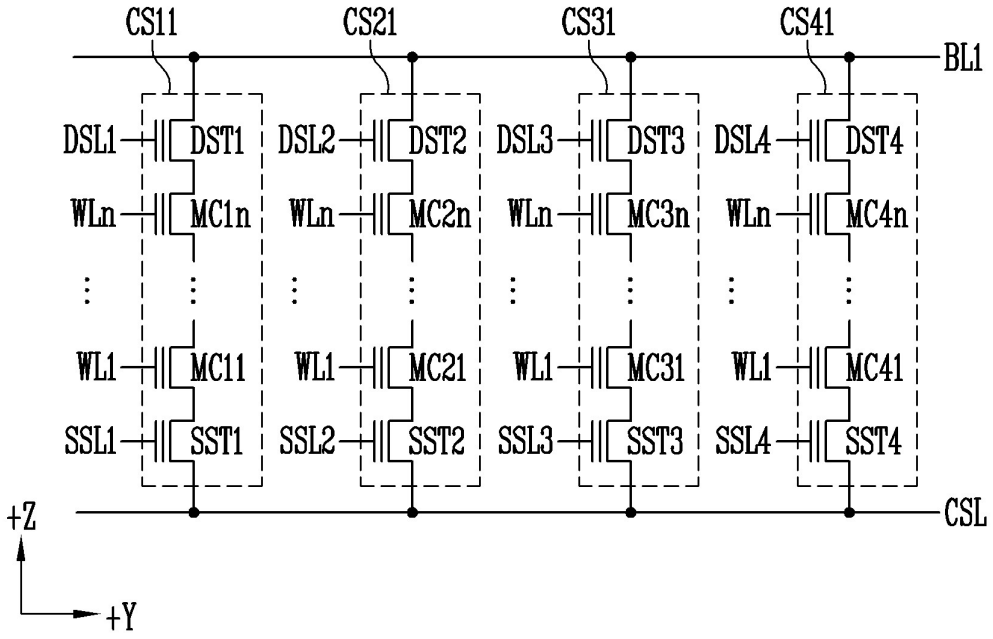

CS11
CS21
CS31
CS41
BL1
DSL1
DST1
DSL2
DST2
DSL3
DST3
DSL4
DST4
WLn
MC1n
MC2n
MC3n
MC4n
WL1
MC11
MC21
MC31
MC41
SSL1
SST1
SSL2
SST2
SSL3
SST3
SSL4
SST4
CSL
+Z
+Y

FIG. 8B

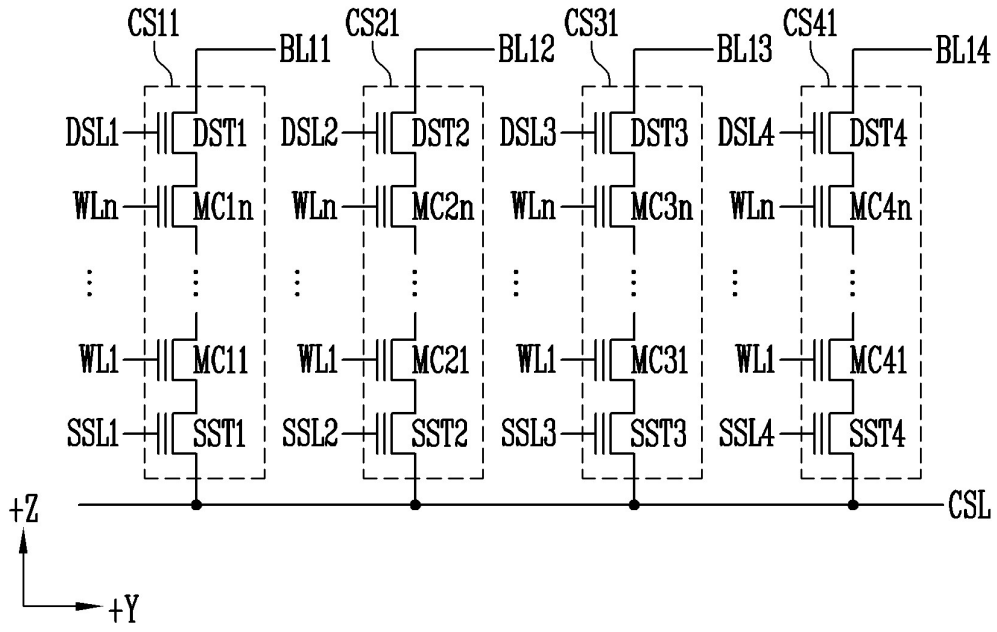

CS11
CS21
CS31
CS41
BL11
BL12
BL13
BL14
DSL1
DSL2
DSL3
DSL4
DST1
DST2
DST3
DST4
WLn
MC1n
MC2n
MC3n
MC4n
WL1
MC11
MC21
MC31
MC41
SSL1
SSL2
SSL3
SSL4
SST1
SST2
SST3
SST4
CSL
+Z
+Y

FIG. 9A

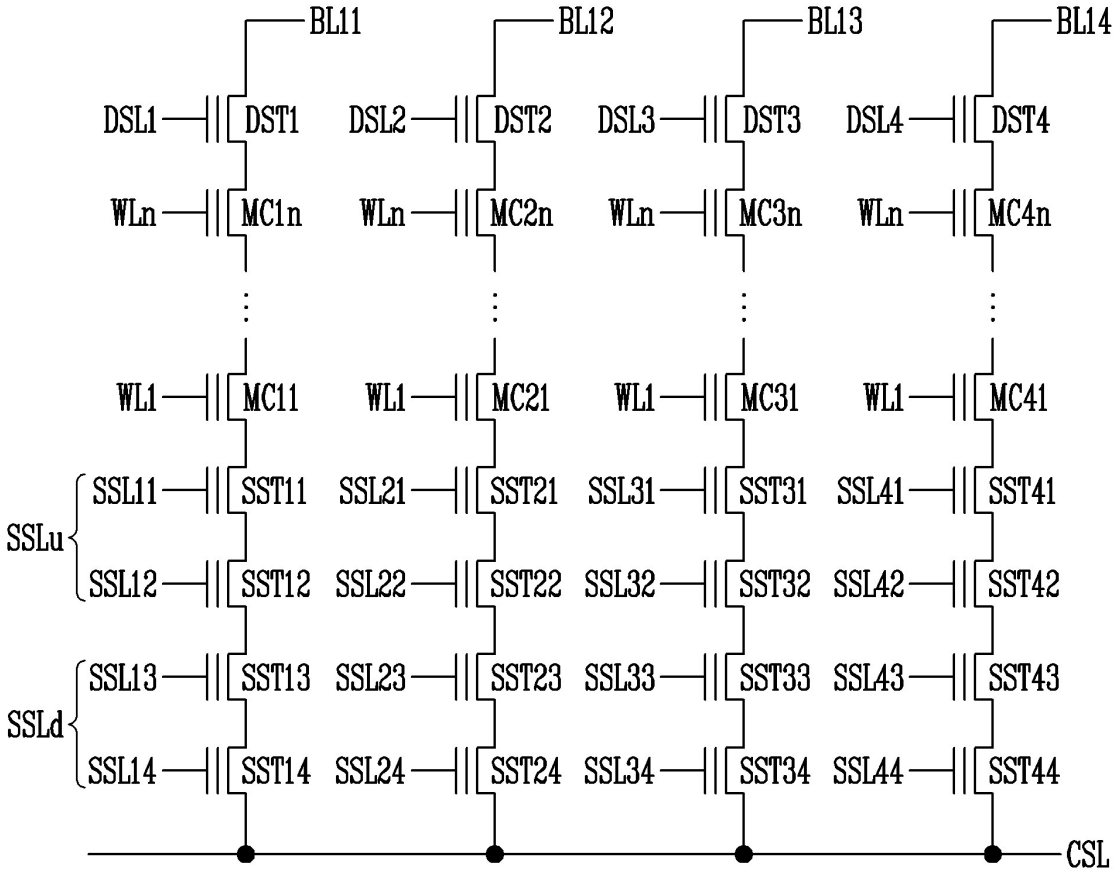

BL11
BL12
BL13
BL14
DSL1
DST1
DSL2
DST2
DSL3
DST3
DSL4
DST4
WLn
MC1n
WLn
MC2n
WLn
MC3n
WLn
MC4n
WL1
MC11
WL1
MC21
WL1
MC31
WL1
MC41
SSLu
SSL11
SST11
SSL21
SST21
SSL31
SST31
SSL41
SST41
SSL12
SST12
SSL22
SST22
SSL32
SST32
SSL42
SST42
SSLd
SSL13
SST13
SSL23
SST23
SSL33
SST33
SSL43
SST43
SSL14
SST14
SSL24
SST24
SSL34
SST34
SSL44
SST44
CSL

FIG. 9B

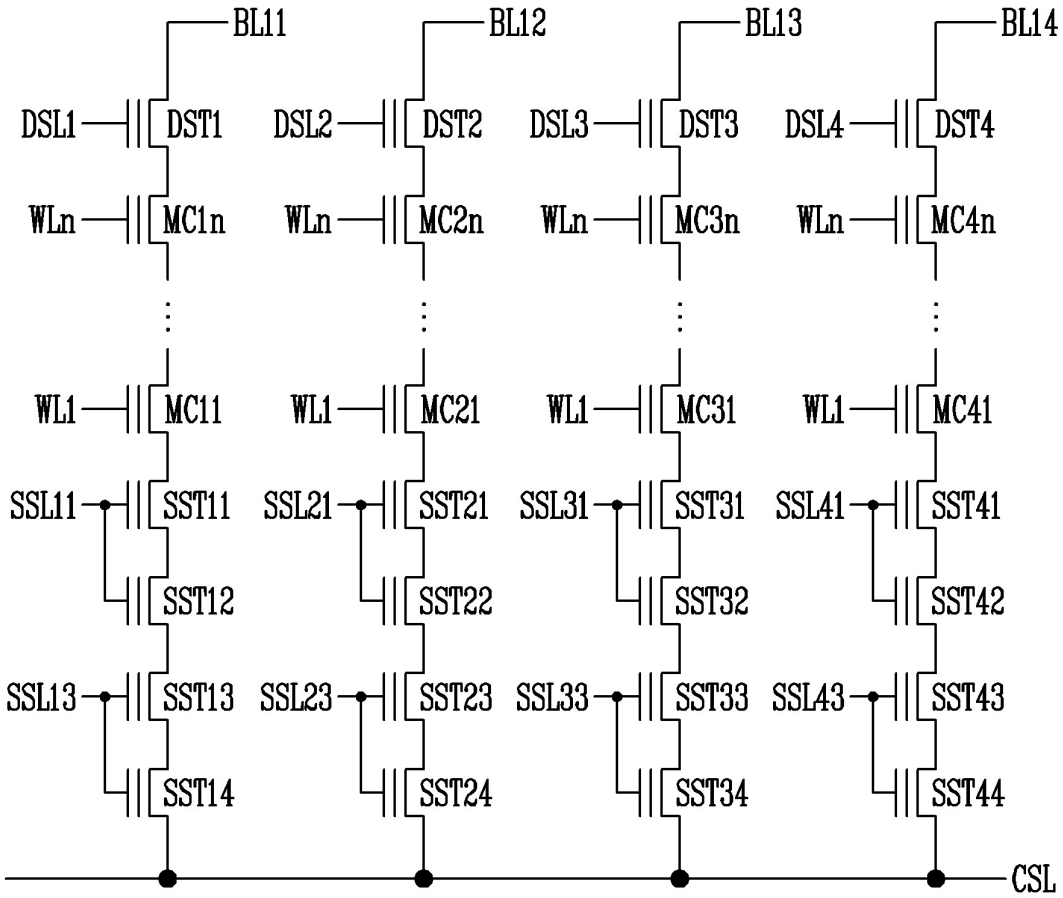

BL11
BL12
BL13
BL14
DSL1
DST1
DSL2
DST2
DSL3
DST3
DSL4
DST4
WLn
MC1n
WLn
MC2n
WLn
MC3n
WLn
MC4n
WL1
MC11
WL1
MC21
WL1
MC31
WL1
MC41
SSL11
SST11
SSL21
SST21
SSL31
SST31
SSL41
SST41
SST12
SST22
SST32
SST42
SSL13
SST13
SSL23
SST23
SSL33
SST33
SSL43
SST43
SST14
SST24
SST34
SST44
CSL

FIG. 9C

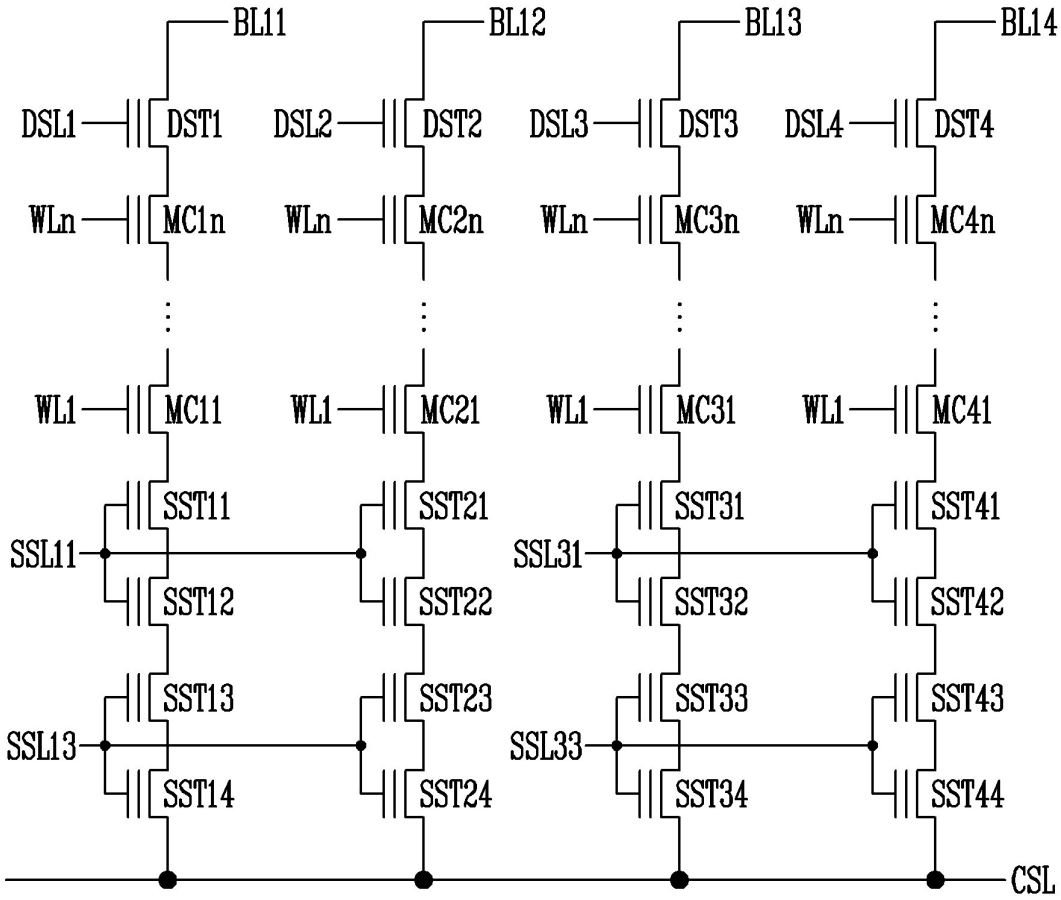

BL11
BL12
BL13
BL14
DSL1
DST1
DSL2
DST2
DSL3
DST3
DSL4
DST4
WLn
MC1n
WLn
MC2n
WLn
MC3n
WLn
MC4n
WL1
MC11
WL1
MC21
WL1
MC31
WL1
MC41
SST11
SST21
SST31
SST41
SSL11
SSL31
SST12
SST22
SST32
SST42
SST13
SST23
SST33
SST43
SSL13
SSL33
SST14
SST24
SST34
SST44
CSL

FIG. 10

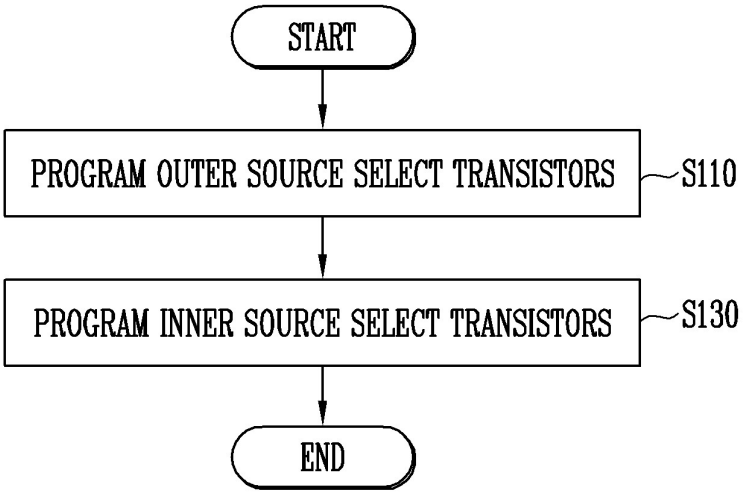

START
PROGRAM OUTER SOURCE SELECT TRANSISTORS
S110
PROGRAM INNER SOURCE SELECT TRANSISTORS
S130
END

FIG. 11A

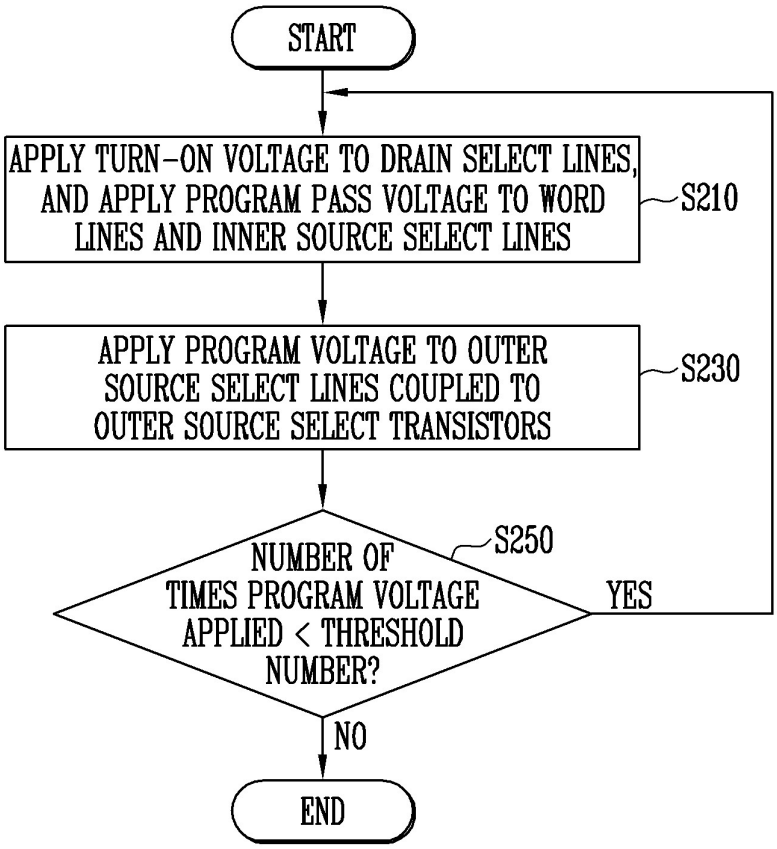

START
APPLY TURN-ON VOLTAGE TO DRAIN SELECT LINES, AND APPLY PROGRAM PASS VOLTAGE TO WORD LINES AND INNER SOURCE SELECT LINES
S210
APPLY PROGRAM VOLTAGE TO OUTER SOURCE SELECT LINES COUPLED TO OUTER SOURCE SELECT TRANSISTORS
S230
NUMBER OF TIMES PROGRAM VOLTAGE APPLIED < THRESHOLD NUMBER?
S250
YES
NO
END

FIG. 11B

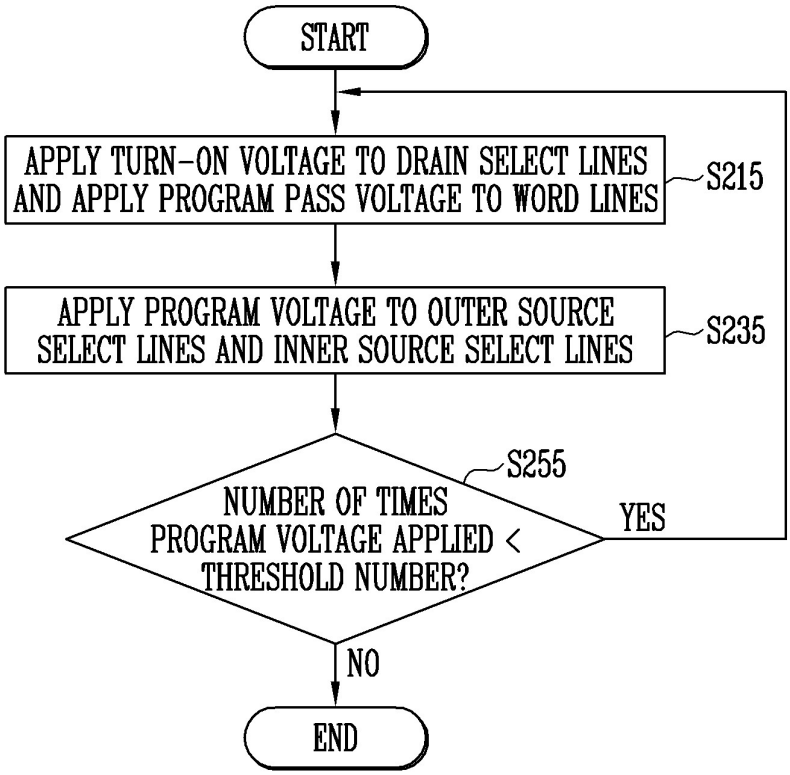

START
APPLY TURN-ON VOLTAGE TO DRAIN SELECT LINES AND APPLY PROGRAM PASS VOLTAGE TO WORD LINES
S215
APPLY PROGRAM VOLTAGE TO OUTER SOURCE SELECT LINES AND INNER SOURCE SELECT LINES
S235
S255
NUMBER OF TIMES PROGRAM VOLTAGE APPLIED < THRESHOLD NUMBER?
YES
NO
END

FIG. 12

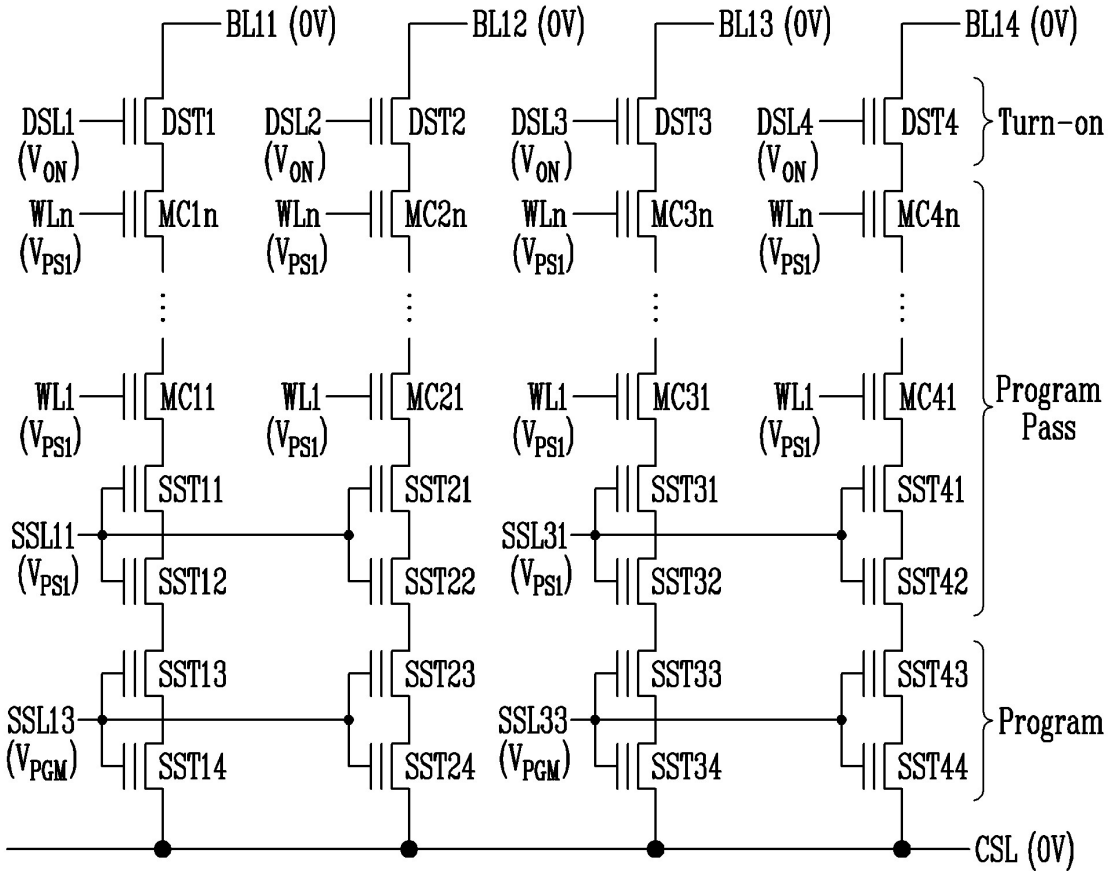

BL11 (0V)
BL12 (0V)
BL13 (0V)
BL14 (0V)
DSL1 (V_{ON})
DST1
DSL2 (V_{ON})
DST2
DSL3 (V_{ON})
DST3
DSL4 (V_{ON})
DST4
Turn-on
WLn (V_{PS1})
MC1n
MC2n
MC3n
MC4n
WL1 (V_{PS1})
MC11
MC21
MC31
MC41
Program Pass
SST11
SST21
SST31
SST41
SSL11 (V_{PS1})
SST12
SST22
SSL31 (V_{PS1})
SST32
SST42
SST13
SST23
SST33
SST43
SSL13 (V_{PGM})
SST14
SST24
SSL33 (V_{PGM})
SST34
SST44
Program
CSL (0V)

FIG. 13

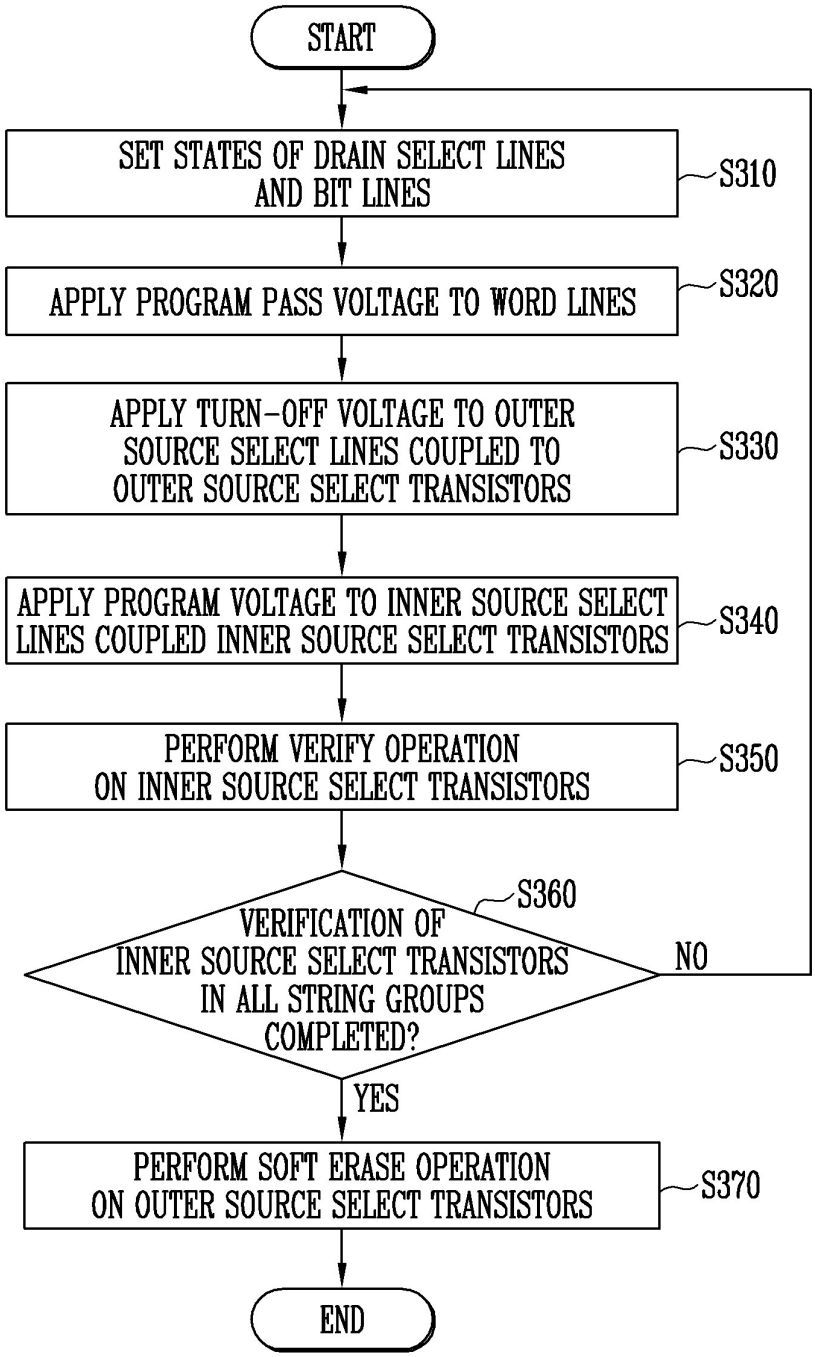

START
SET STATES OF DRAIN SELECT LINES AND BIT LINES
S310
APPLY PROGRAM PASS VOLTAGE TO WORD LINES
S320
APPLY TURN-OFF VOLTAGE TO OUTER SOURCE SELECT LINES COUPLED TO OUTER SOURCE SELECT TRANSISTORS
S330
APPLY PROGRAM VOLTAGE TO INNER SOURCE SELECT LINES COUPLED INNER SOURCE SELECT TRANSISTORS
S340
PERFORM VERIFY OPERATION ON INNER SOURCE SELECT TRANSISTORS
S350
S360
VERIFICATION OF INNER SOURCE SELECT TRANSISTORS IN ALL STRING GROUPS COMPLETED?
NO
YES
PERFORM SOFT ERASE OPERATION ON OUTER SOURCE SELECT TRANSISTORS
S370
END

FIG. 14

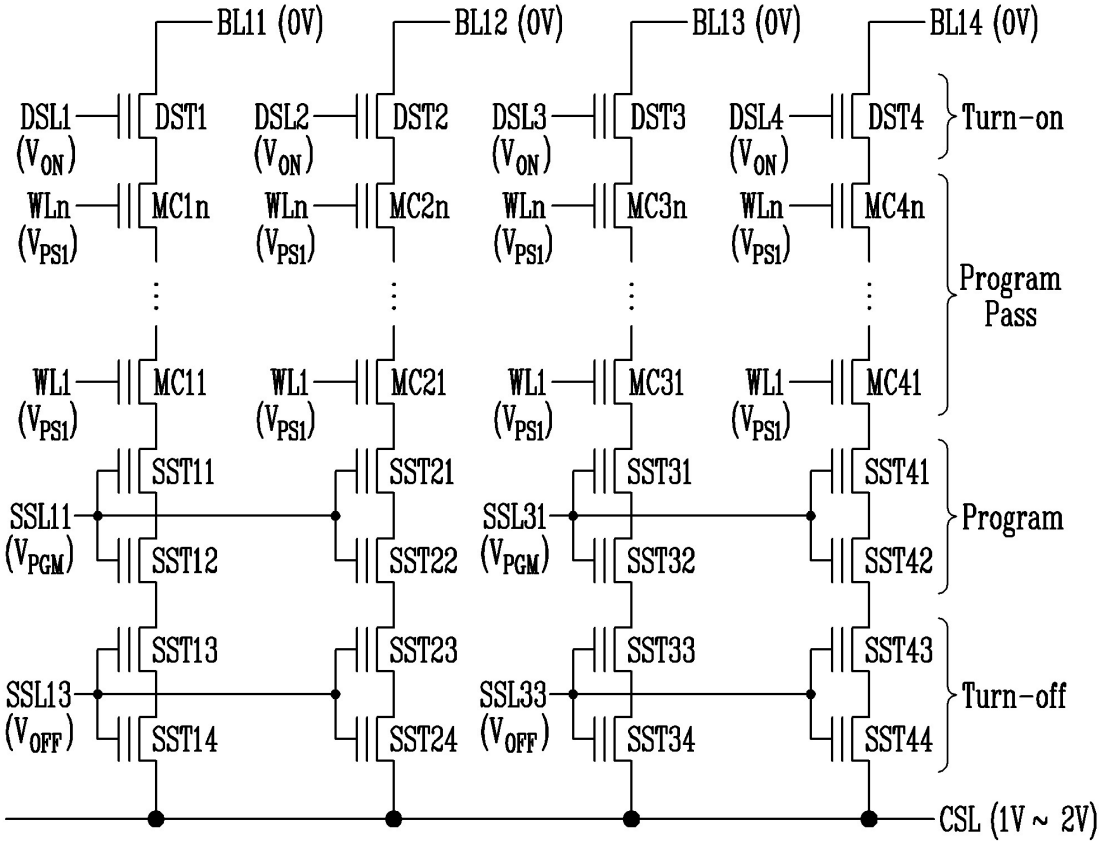

BL11 (0V)
BL12 (0V)
BL13 (0V)
BL14 (0V)
DSL1 (V_{ON})
DSL2 (V_{ON})
DSL3 (V_{ON})
DSL4 (V_{ON})
DST1
DST2
DST3
DST4
Turn-on
WLn (V_{PS1})
MC1n
MC2n
MC3n
MC4n
Program Pass
WL1 (V_{PS1})
MC11
MC21
MC31
MC41
SST11
SST21
SST31
SST41
SSL11 (V_{PGM})
SSL31 (V_{PGM})
SST12
SST22
SST32
SST42
Program
SST13
SST23
SST33
SST43
SSL13 (V_{OFF})
SSL33 (V_{OFF})
SST14
SST24
SST34
SST44
Turn-off
CSL (1V ~ 2V)

FIG. 15

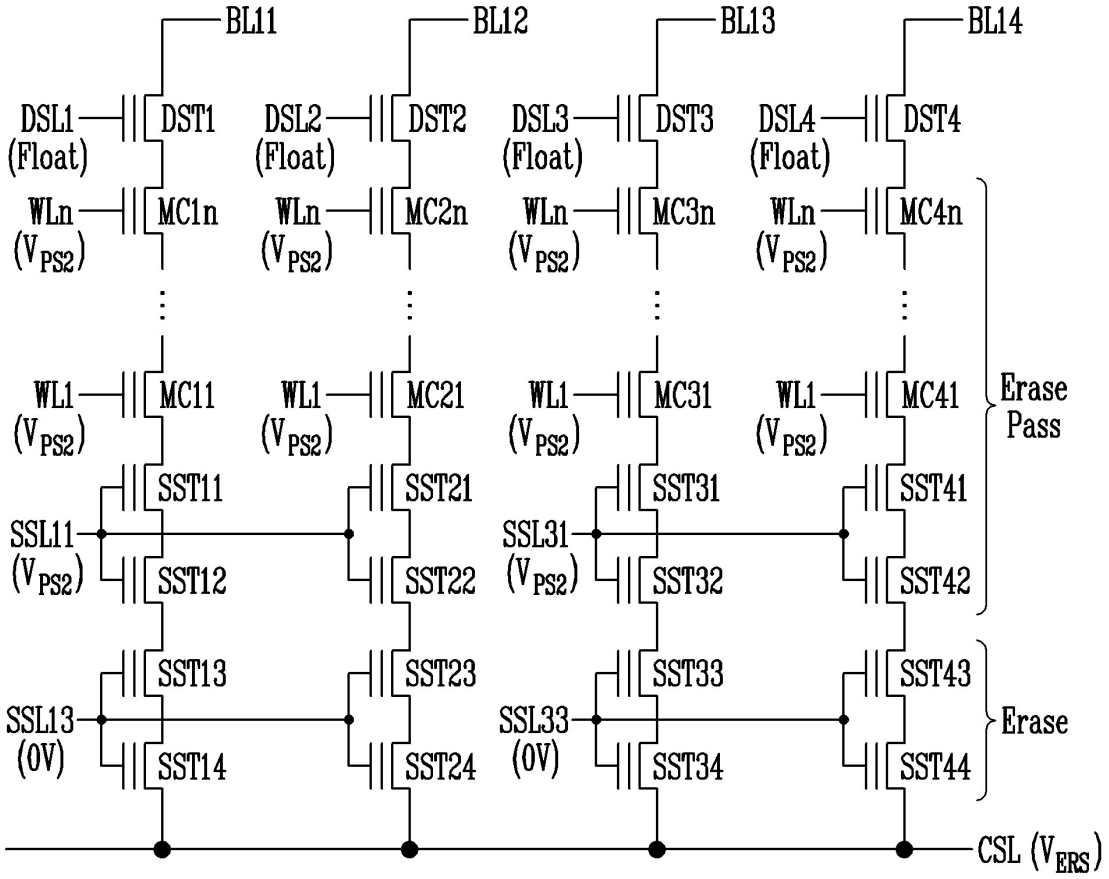

BL11
BL12
BL13
BL14
DSL1 (Float)
DSL2 (Float)
DSL3 (Float)
DSL4 (Float)
DST1
DST2
DST3
DST4
WLn (V_{PS2})
MC1n
MC2n
MC3n
MC4n
WL1 (V_{PS2})
MC11
MC21
MC31
MC41
Erase Pass
SST11
SST21
SST31
SST41
SSL11 (V_{PS2})
SSL31 (V_{PS2})
SST12
SST22
SST32
SST42
SST13
SST23
SST33
SST43
SSL13 (0V)
SSL33 (0V)
Erase
SST14
SST24
SST34
SST44
CSL (V_{ERS})

FIG. 16

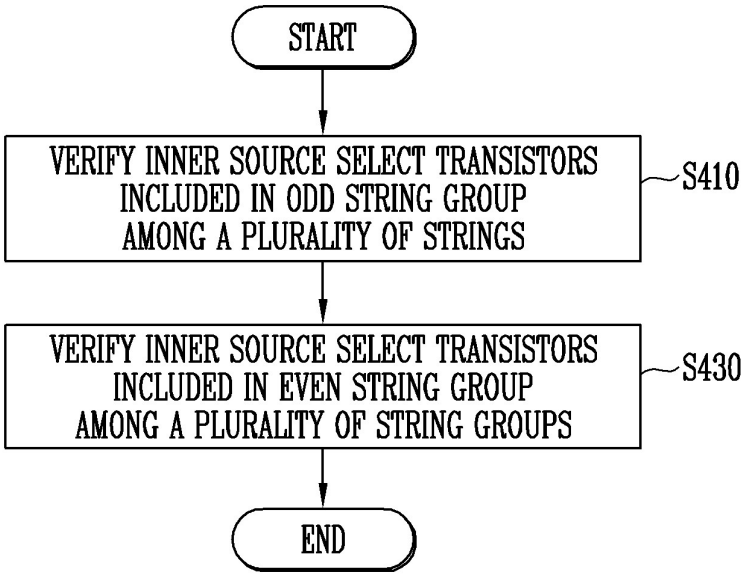

START
VERIFY INNER SOURCE SELECT TRANSISTORS INCLUDED IN ODD STRING GROUP AMONG A PLURALITY OF STRINGS
S410
VERIFY INNER SOURCE SELECT TRANSISTORS INCLUDED IN EVEN STRING GROUP AMONG A PLURALITY OF STRING GROUPS
S430
END

FIG. 17

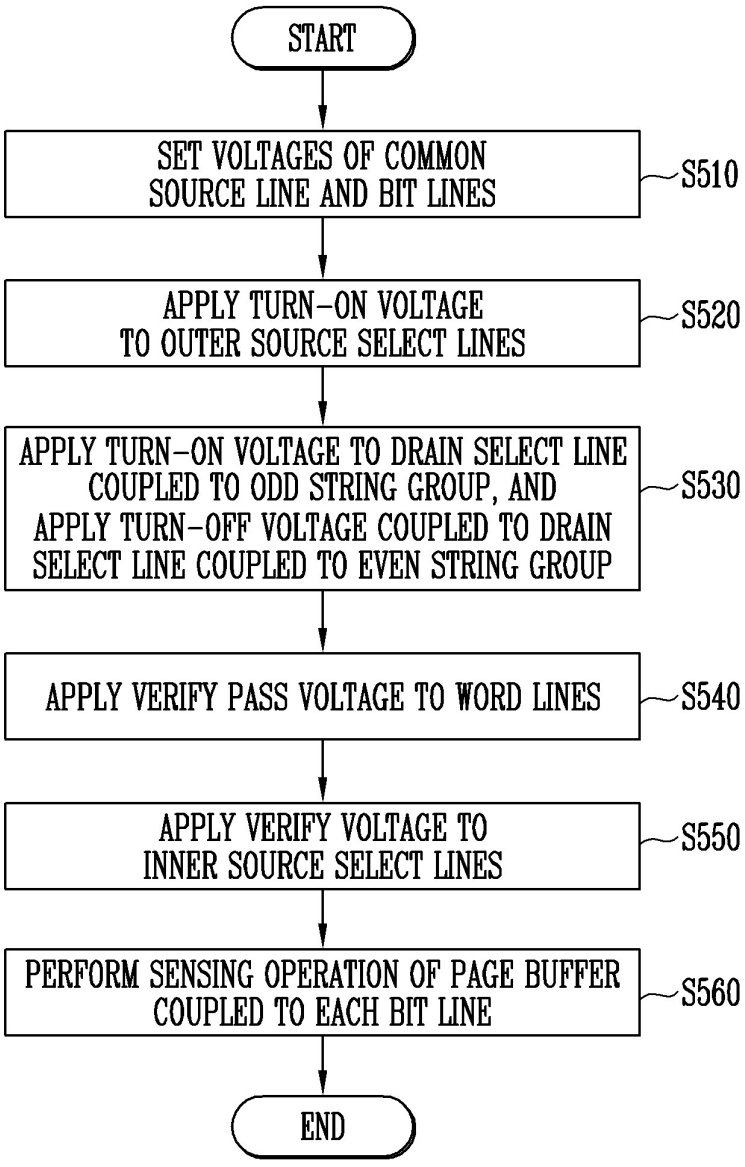

START
SET VOLTAGES OF COMMON SOURCE LINE AND BIT LINES
S510
APPLY TURN-ON VOLTAGE TO OUTER SOURCE SELECT LINES
S520
APPLY TURN-ON VOLTAGE TO DRAIN SELECT LINE COUPLED TO ODD STRING GROUP, AND APPLY TURN-OFF VOLTAGE COUPLED TO DRAIN SELECT LINE COUPLED TO EVEN STRING GROUP
S530
APPLY VERIFY PASS VOLTAGE TO WORD LINES
S540
APPLY VERIFY VOLTAGE TO INNER SOURCE SELECT LINES
S550
PERFORM SENSING OPERATION OF PAGE BUFFER COUPLED TO EACH BIT LINE
S560
END

FIG. 18A

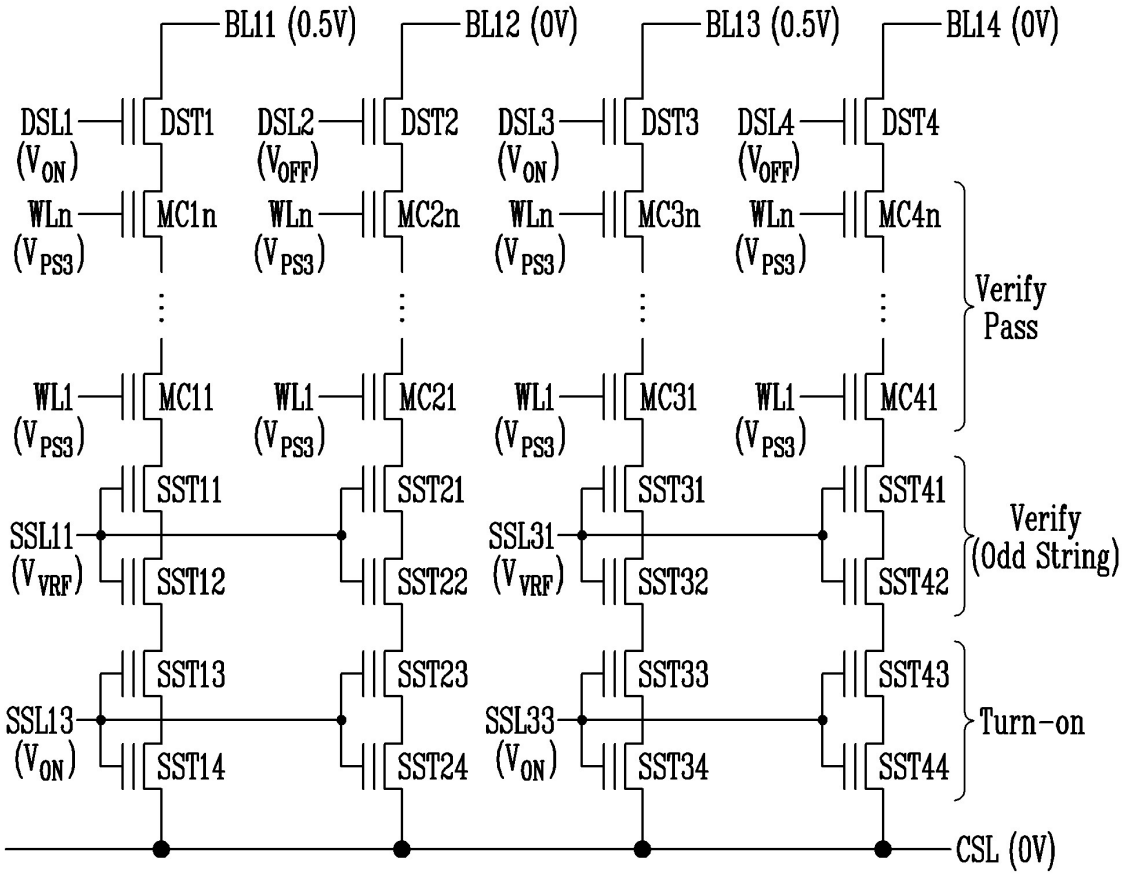

BL11 (0.5V)
BL12 (0V)
BL13 (0.5V)
BL14 (0V)
DSL1 (V_{ON})
DSL2 (V_{OFF})
DSL3 (V_{ON})
DSL4 (V_{OFF})
DST1
DST2
DST3
DST4
WLn (V_{PS3})
MC1n
MC2n
MC3n
MC4n
Verify Pass
WL1 (V_{PS3})
MC11
MC21
MC31
MC41
SST11
SST21
SST31
SST41
SSL11 (V_{VRF})
SSL31 (V_{VRF})
SST12
SST22
SST32
SST42
Verify (Odd String)
SST13
SST23
SST33
SST43
SSL13 (V_{ON})
SSL33 (V_{ON})
SST14
SST24
SST34
SST44
Turn-on
CSL (0V)

FIG. 18B

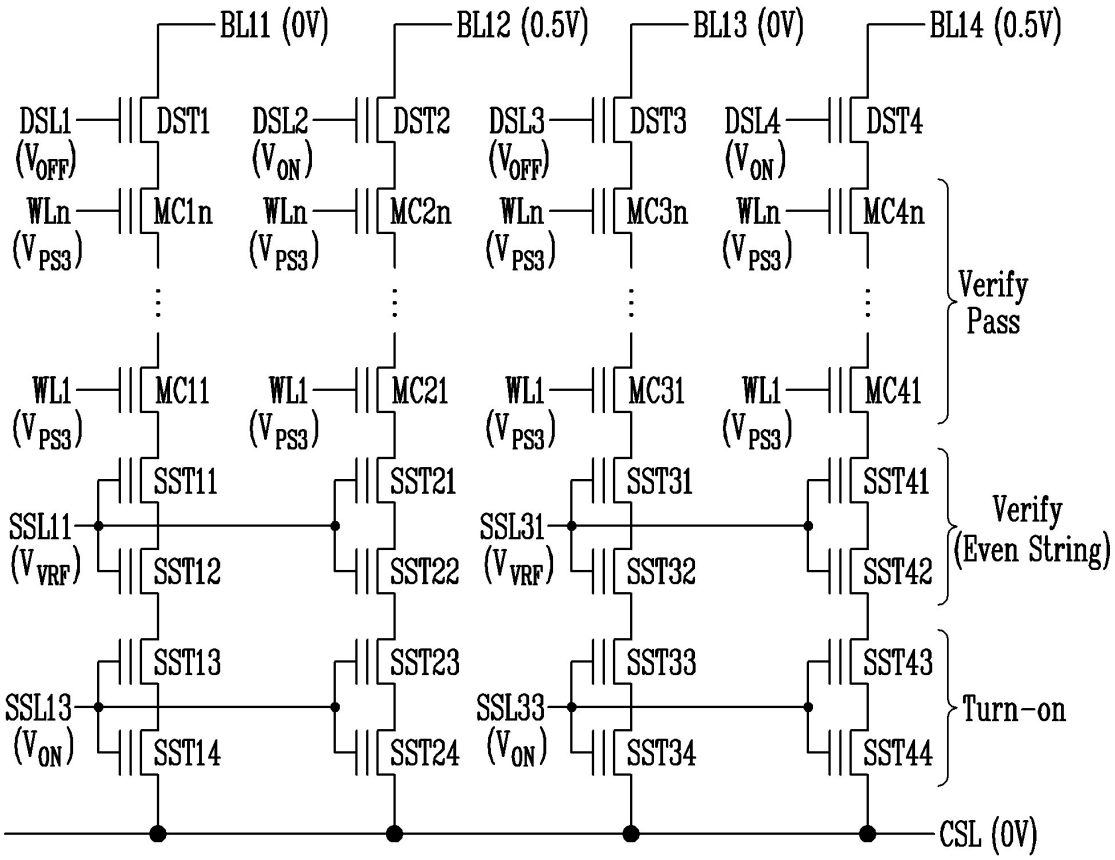

BL11 (0V)
BL12 (0.5V)
BL13 (0V)
BL14 (0.5V)
DSL1 (V_{OFF})
DSL2 (V_{ON})
DSL3 (V_{OFF})
DSL4 (V_{ON})
DST1
DST2
DST3
DST4
WLn (V_{PS3})
MC1n
MC2n
MC3n
MC4n
WL1 (V_{PS3})
MC11
MC21
MC31
MC41
Verify Pass
SST11
SST21
SST31
SST41
SSL11 (V_{VRF})
SSL31 (V_{VRF})
SST12
SST22
SST32
SST42
Verify (Even String)
SST13
SST23
SST33
SST43
SSL13 (V_{ON})
SSL33 (V_{ON})
SST14
SST24
SST34
SST44
Turn-on
CSL (0V)

FIG. 19

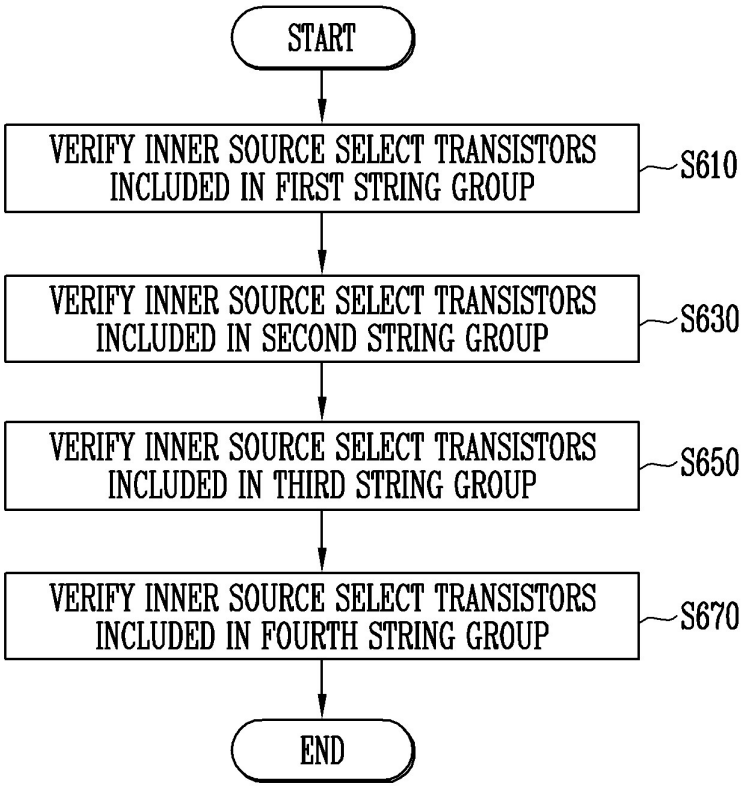

START
VERIFY INNER SOURCE SELECT TRANSISTORS INCLUDED IN FIRST STRING GROUP
S610
VERIFY INNER SOURCE SELECT TRANSISTORS INCLUDED IN SECOND STRING GROUP
S630
VERIFY INNER SOURCE SELECT TRANSISTORS INCLUDED IN THIRD STRING GROUP
S650
VERIFY INNER SOURCE SELECT TRANSISTORS INCLUDED IN FOURTH STRING GROUP
S670
END

FIG. 20

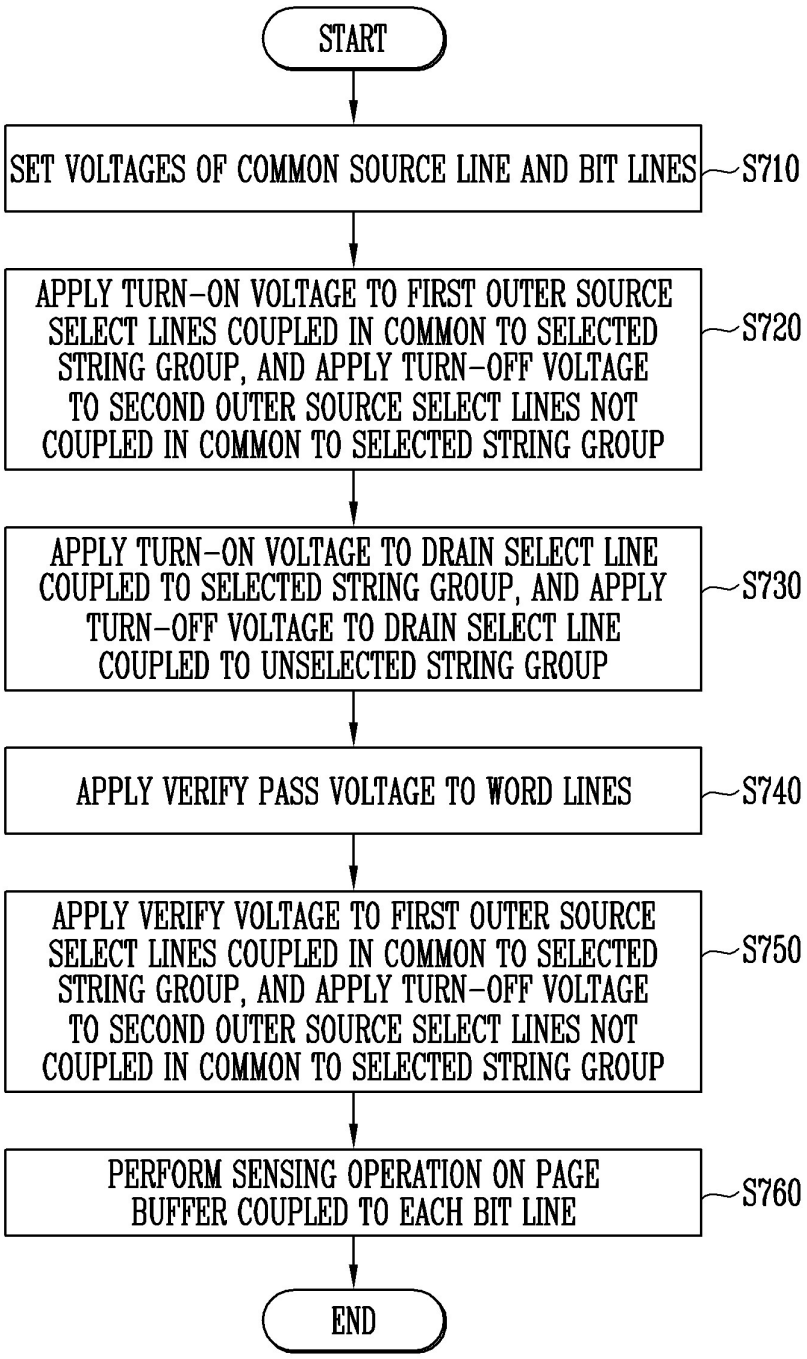

START
SET VOLTAGES OF COMMON SOURCE LINE AND BIT LINES
S710
APPLY TURN-ON VOLTAGE TO FIRST OUTER SOURCE SELECT LINES COUPLED IN COMMON TO SELECTED STRING GROUP, AND APPLY TURN-OFF VOLTAGE TO SECOND OUTER SOURCE SELECT LINES NOT COUPLED IN COMMON TO SELECTED STRING GROUP
S720
APPLY TURN-ON VOLTAGE TO DRAIN SELECT LINE COUPLED TO SELECTED STRING GROUP, AND APPLY TURN-OFF VOLTAGE TO DRAIN SELECT LINE COUPLED TO UNSELECTED STRING GROUP
S730
APPLY VERIFY PASS VOLTAGE TO WORD LINES
S740
APPLY VERIFY VOLTAGE TO FIRST OUTER SOURCE SELECT LINES COUPLED IN COMMON TO SELECTED STRING GROUP, AND APPLY TURN-OFF VOLTAGE TO SECOND OUTER SOURCE SELECT LINES NOT COUPLED IN COMMON TO SELECTED STRING GROUP
S750
PERFORM SENSING OPERATION ON PAGE BUFFER COUPLED TO EACH BIT LINE
S760
END

FIG. 21A

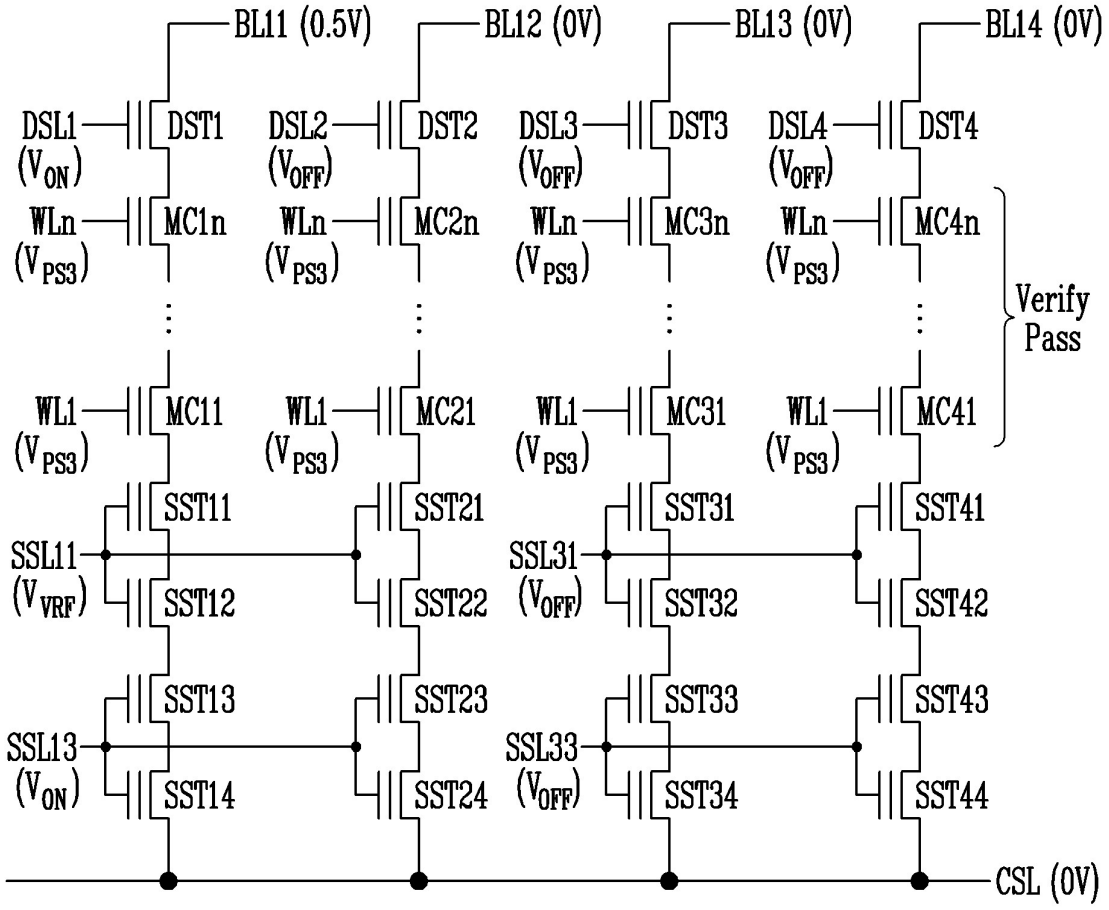

BL11 (0.5V)
BL12 (0V)
BL13 (0V)
BL14 (0V)
DSL1 (V_{ON})
DSL2 (V_{OFF})
DSL3 (V_{OFF})
DSL4 (V_{OFF})
DST1
DST2
DST3
DST4
WLn (V_{PS3})
MC1n
MC2n
MC3n
MC4n
Verify Pass
WL1 (V_{PS3})
MC11
MC21
MC31
MC41
SST11
SST21
SST31
SST41
SSL11 (V_{VRF})
SSL31 (V_{OFF})
SST12
SST22
SST32
SST42
SST13
SST23
SST33
SST43
SSL13 (V_{ON})
SSL33 (V_{OFF})
SST14
SST24
SST34
SST44
CSL (0V)

FIG. 21B

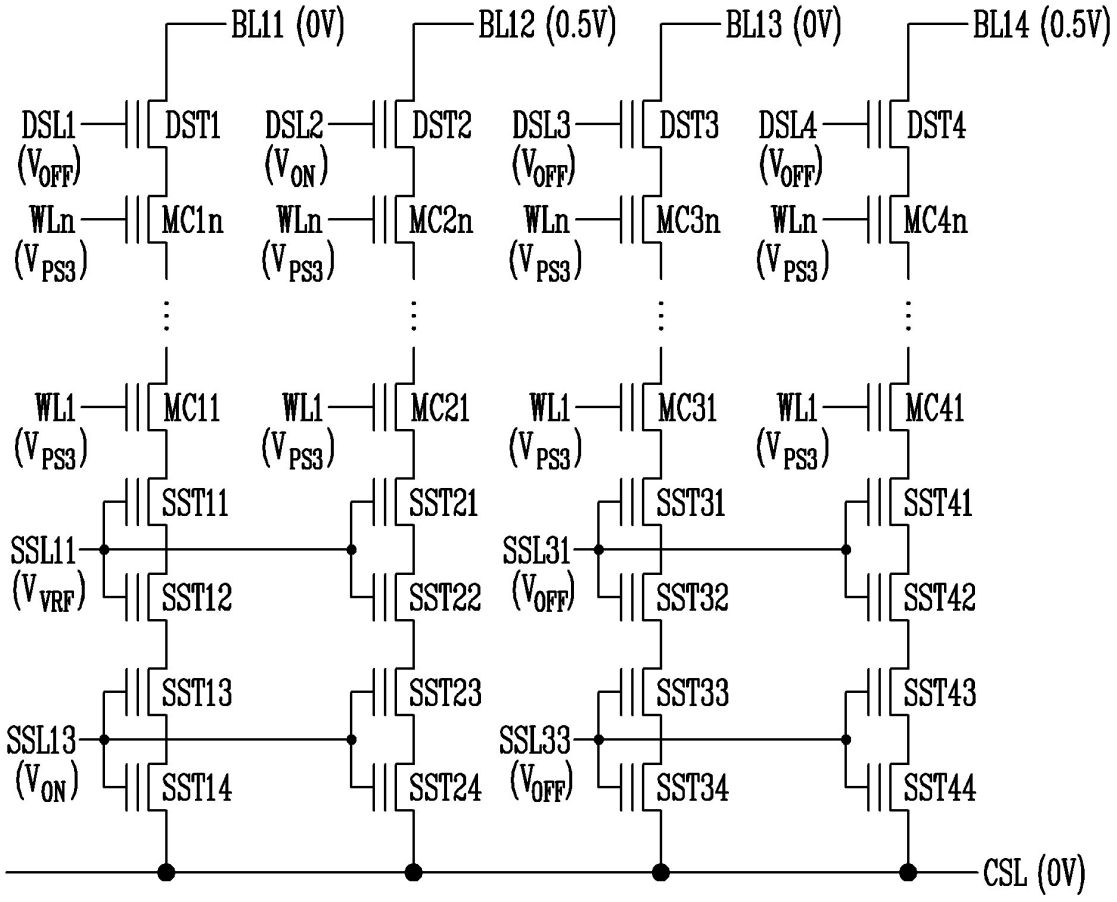

BL11 (0V)
BL12 (0.5V)
BL13 (0V)
BL14 (0.5V)
DSL1 (V_{OFF})
DSL2 (V_{ON})
DSL3 (V_{OFF})
DSL4 (V_{OFF})
DST1
DST2
DST3
DST4
WLn (V_{PS3})
MC1n
MC2n
MC3n
MC4n
WL1 (V_{PS3})
MC11
MC21
MC31
MC41
SST11
SST21
SST31
SST41
SSL11 (V_{VRF})
SSL31 (V_{OFF})
SST12
SST22
SST32
SST42
SST13
SST23
SST33
SST43
SSL13 (V_{ON})
SSL33 (V_{OFF})
SST14
SST24
SST34
SST44
CSL (0V)

FIG. 22

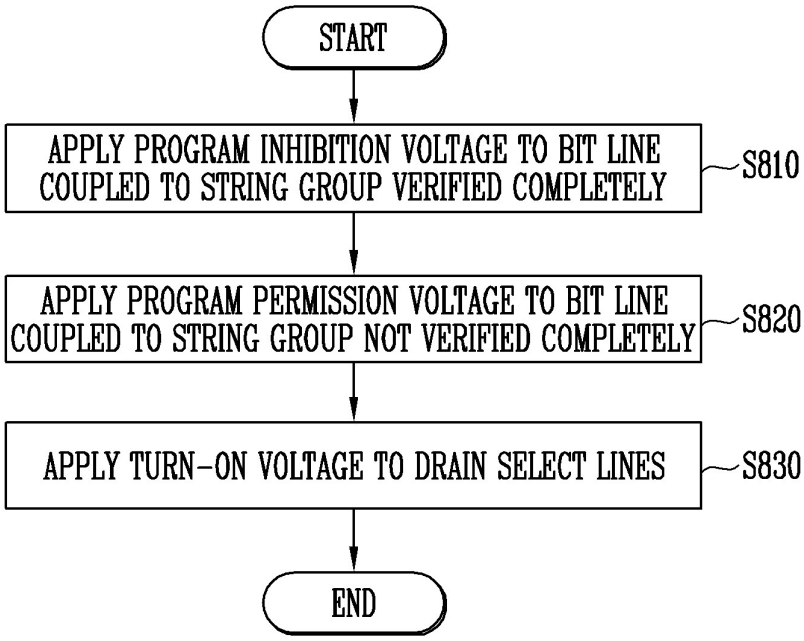

START
APPLY PROGRAM INHIBITION VOLTAGE TO BIT LINE COUPLED TO STRING GROUP VERIFIED COMPLETELY
S810
APPLY PROGRAM PERMISSION VOLTAGE TO BIT LINE COUPLED TO STRING GROUP NOT VERIFIED COMPLETELY
S820
APPLY TURN-ON VOLTAGE TO DRAIN SELECT LINES
S830
END

FIG. 23

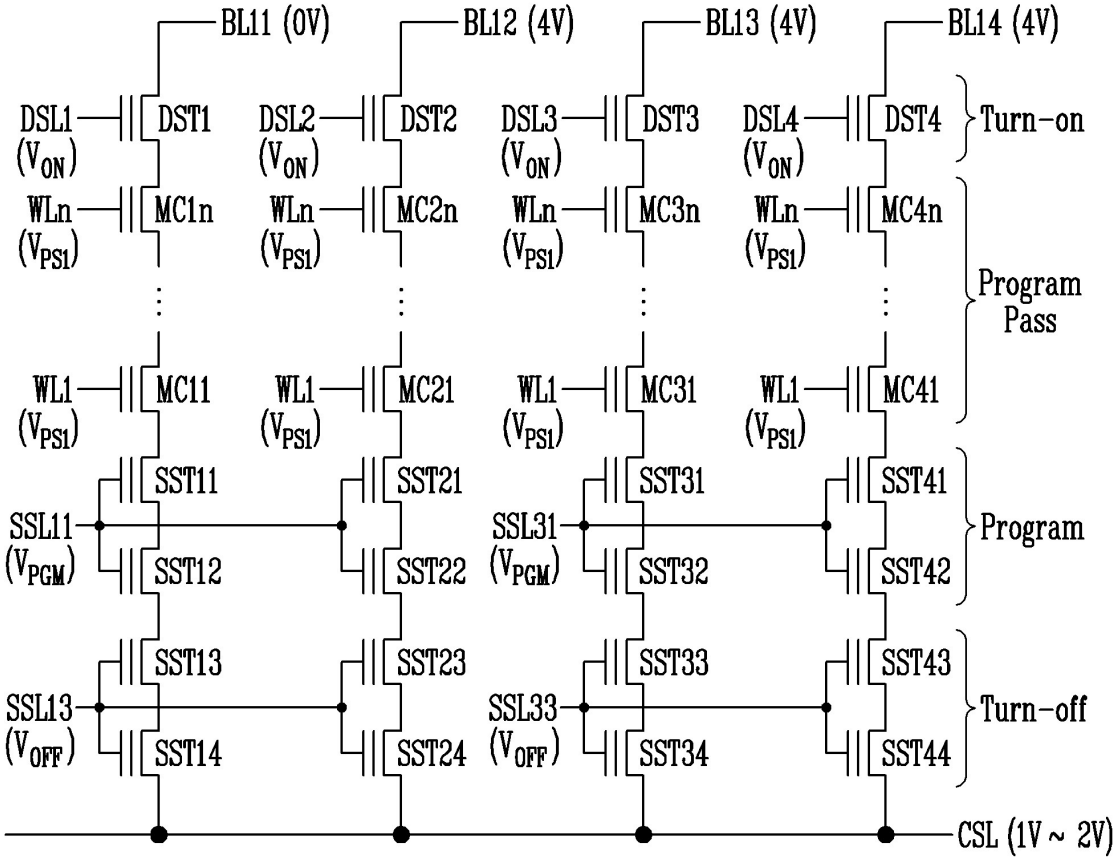

BL11 (0V)
BL12 (4V)
BL13 (4V)
BL14 (4V)
DSL1 (V_{ON})
DST1
DSL2 (V_{ON})
DST2
DSL3 (V_{ON})
DST3
DSL4 (V_{ON})
DST4
Turn-on
WLn (V_{PS1})
MC1n
MC2n
MC3n
MC4n
Program Pass
WL1 (V_{PS1})
MC11
MC21
MC31
MC41
SST11
SST21
SST31
SST41
SSL11 (V_{PGM})
SST12
SST22
SSL31 (V_{PGM})
SST32
SST42
Program
SST13
SST23
SST33
SST43
SSL13 (V_{OFF})
SST14
SST24
SSL33 (V_{OFF})
SST34
SST44
Turn-off
CSL (1V ~ 2V)

FIG. 24

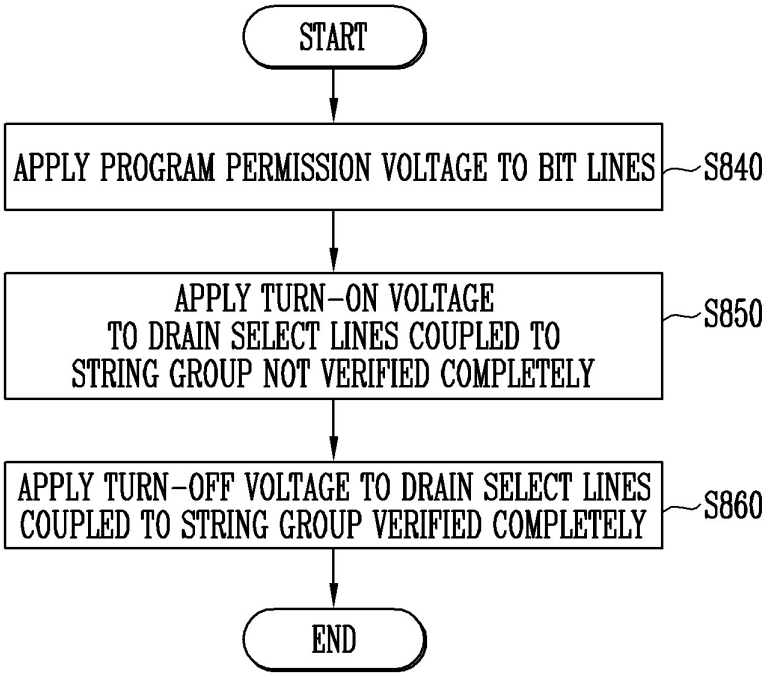

START
APPLY PROGRAM PERMISSION VOLTAGE TO BIT LINES
S840
APPLY TURN-ON VOLTAGE TO DRAIN SELECT LINES COUPLED TO STRING GROUP NOT VERIFIED COMPLETELY
S850
APPLY TURN-OFF VOLTAGE TO DRAIN SELECT LINES COUPLED TO STRING GROUP VERIFIED COMPLETELY
S860
END

FIG. 25

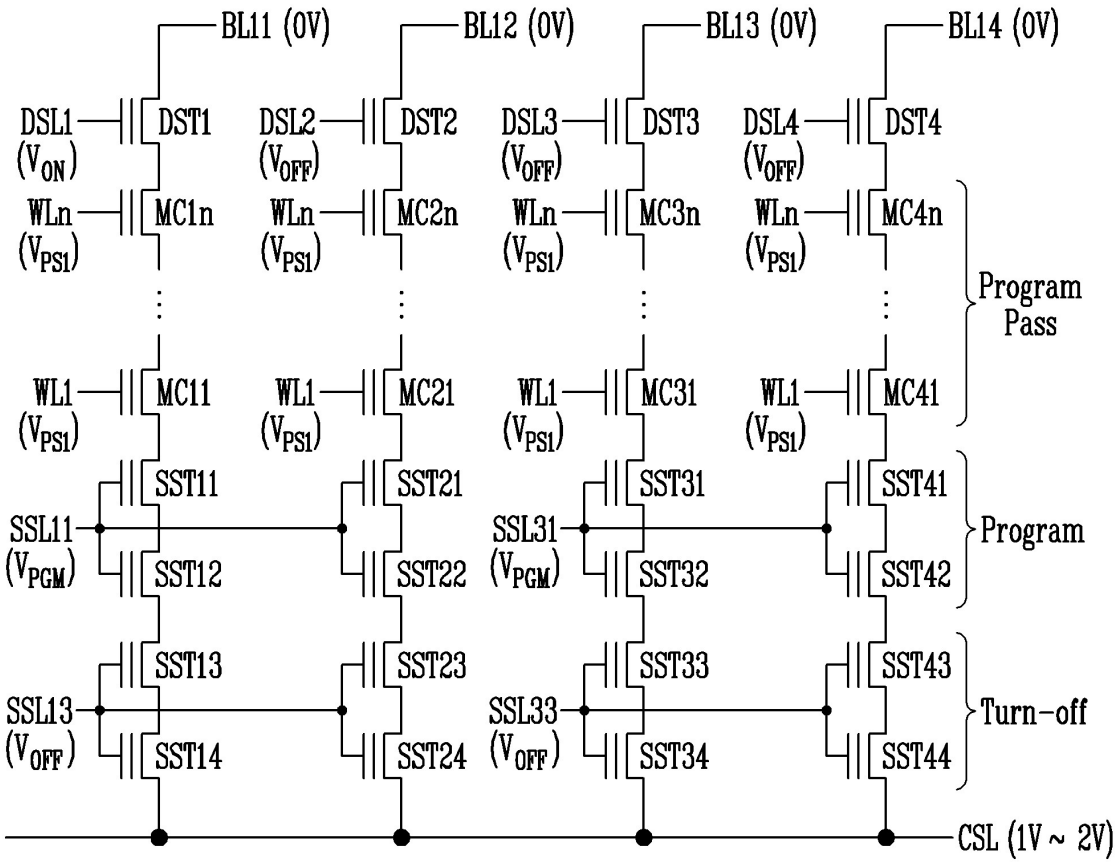

BL11 (0V)
BL12 (0V)
BL13 (0V)
BL14 (0V)
DSL1 (V_{ON})
DSL2 (V_{OFF})
DSL3 (V_{OFF})
DSL4 (V_{OFF})
DST1
DST2
DST3
DST4
WLn (V_{PS1})
MC1n
MC2n
MC3n
MC4n
Program Pass
WL1 (V_{PS1})
MC11
MC21
MC31
MC41
SST11
SST21
SST31
SST41
SSL11 (V_{PGM})
SSL31 (V_{PGM})
SST12
SST22
SST32
SST42
Program
SST13
SST23
SST33
SST43
SSL13 (V_{OFF})
SSL33 (V_{OFF})
SST14
SST24
SST34
SST44
Turn-off
CSL (1V ~ 2V)

FIG. 26

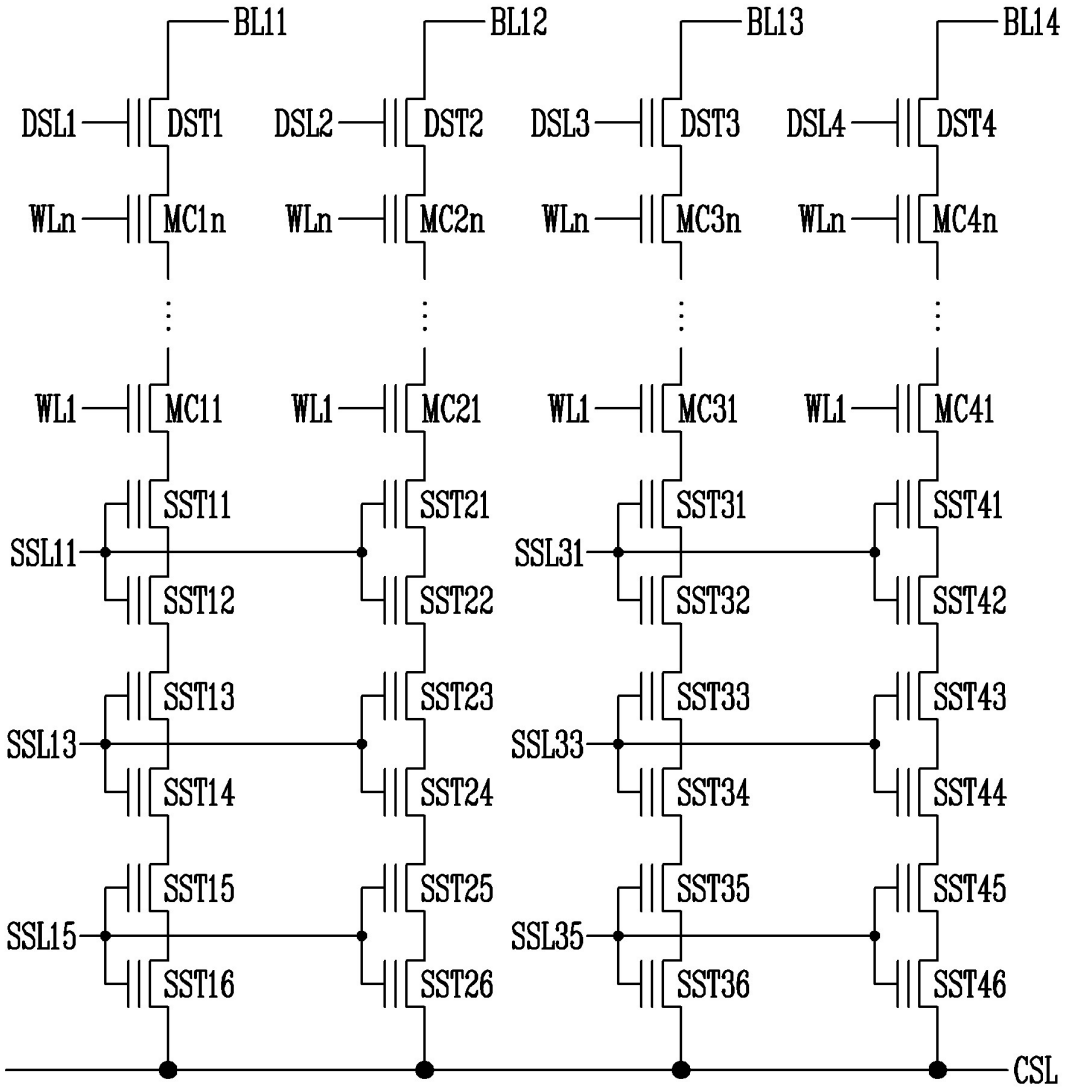

BL11
BL12
BL13
BL14
DSL1
DST1
DSL2
DST2
DSL3
DST3
DSL4
DST4
WLn
MC1n
WLn
MC2n
WLn
MC3n
WLn
MC4n
WL1
MC11
WL1
MC21
WL1
MC31
WL1
MC41
SST11
SST21
SST31
SST41
SSL11
SSL31
SST12
SST22
SST32
SST42
SST13
SST23
SST33
SST43
SSL13
SSL33
SST14
SST24
SST34
SST44
SST15
SST25
SST35
SST45
SSL15
SSL35
SST16
SST26
SST36
SST46
CSL

FIG. 27

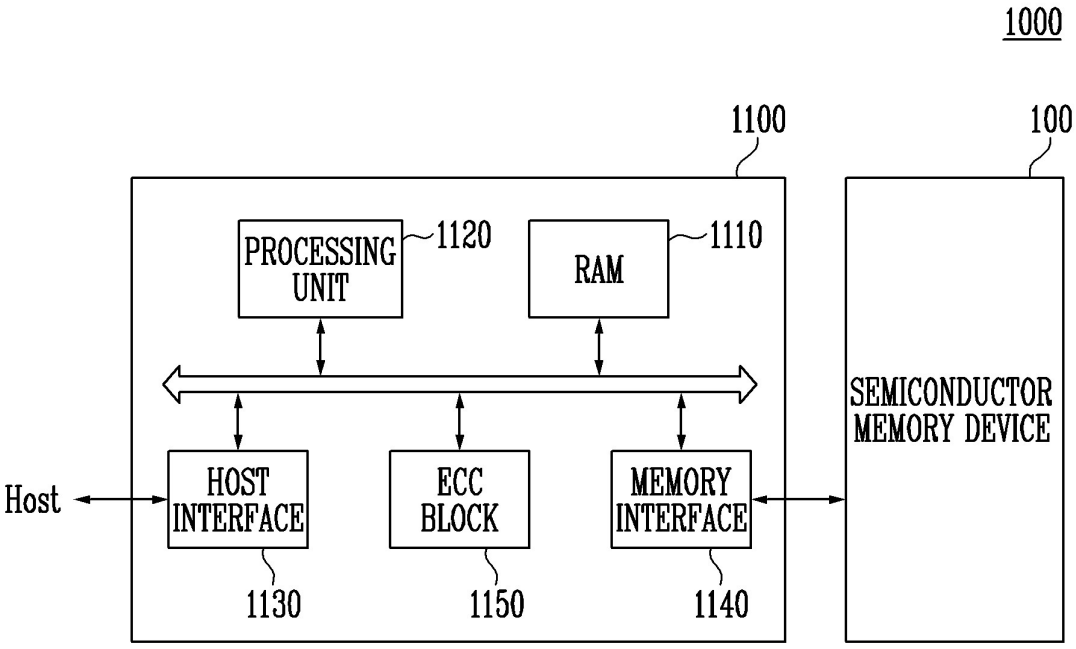

1000
1100
100
PROCESSING UNIT
1120
RAM
1110
SEMICONDUCTOR MEMORY DEVICE
Host
HOST INTERFACE
ECC BLOCK
MEMORY INTERFACE
1130
1150
1140

FIG. 28

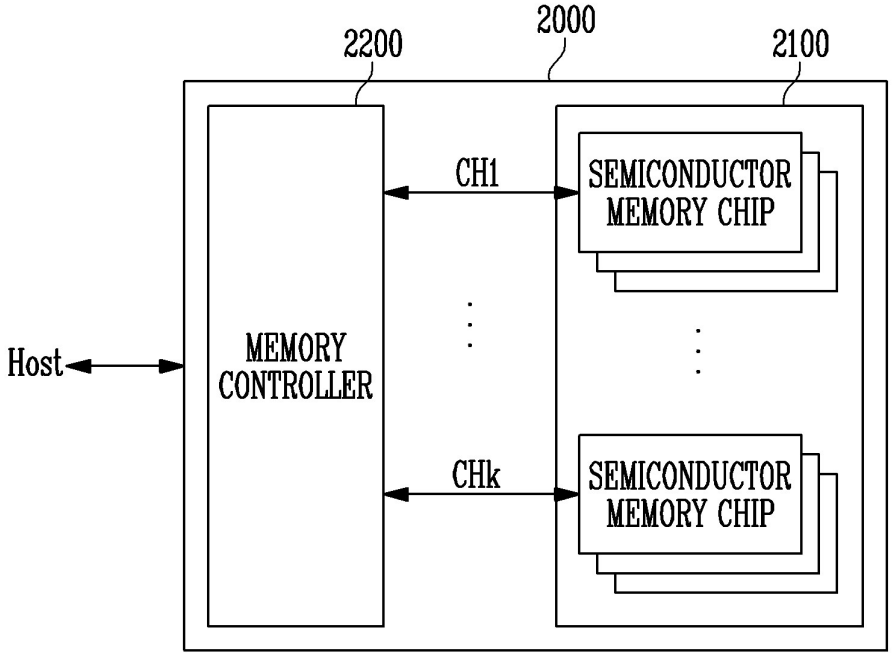
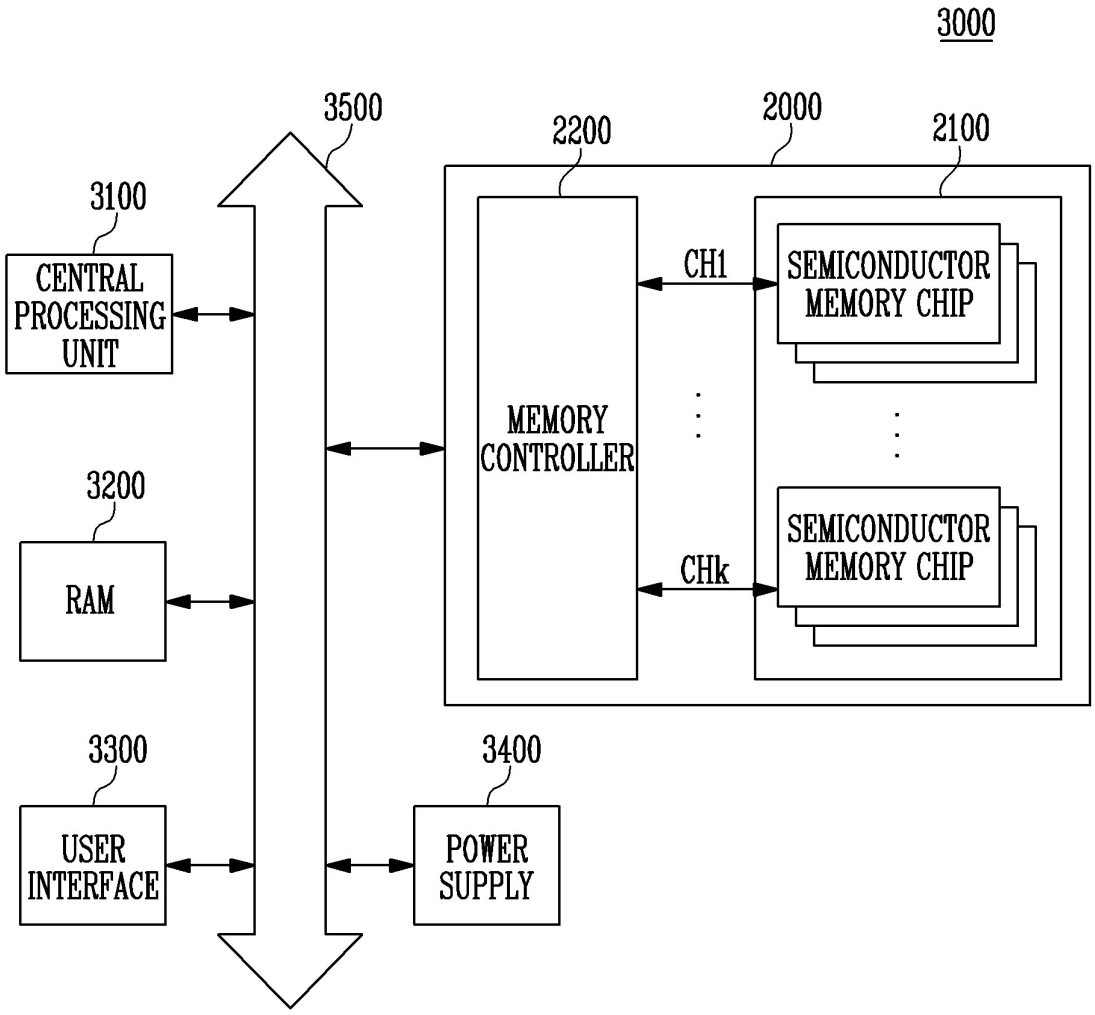

2000
2200
2100
CH1
SEMICONDUCTOR MEMORY CHIP
Host
MEMORY CONTROLLER
CHk
SEMICONDUCTOR MEMORY CHIP

FIG. 29


3000
3500
2200
2000
2100
3100
CENTRAL PROCESSING UNIT
CH1
SEMICONDUCTOR MEMORY CHIP
MEMORY CONTROLLER
3200
RAM
CHk
SEMICONDUCTOR MEMORY CHIP
3300
3400
USER INTERFACE
POWER SUPPLY