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D E S C R I P T I O N

REFRACTORY METAL CAPPED LOW RESISTIVITY METAL CONDUCTOR LINES AND VIAS FORMED USING PVD AND CVD

The present invention generally relates to the manufacture of electrical conductor lines and vias that interconnect circuits on substrates such as semiconductors and related packages and, more particularly, to a low cost method of filling seams or holes in substrates using a combination of a low resistivity metal deposited by physical vapor deposition (PVD) and a refractory metal deposited by chemical vapor deposition (CVD). The invention has particular application in submicron circuit manufacture.

Low resistivity metals such as aluminum and copper and their binary and ternary alloys have been widely explored as fine line interconnects in semiconductor manufacturing. Typical examples of fine line interconnect metals include Al_xCu_y, where the sum of x and y is equal to one and both x and y are greater than or equal to zero and less than or equal to one, ternary alloys such as Al-Pd-Cu and Al-Pd-Nb, Al-Cu-Si, and other similar low resistivity metal based alloys. Today's emphasis on scaling down line width dimensions in very large scale integrated (VLSI) circuitry manufacture has led to reliability problems including inadequate isolation, electromigration, and planarization.

The IBM Technical Disclosure Bulletin to Ahn et al., Vol. 33, No. 5, October 1990, pages 217-218, discloses tungsten wrapped copper conductors and via holes

fabricated by selective deposition using a mixture of WF_6 and SiH_4 in the presence of hydrogen. Encapsulated interconnects like those of Ahn et al. have significantly higher resistance to electromigration and the small grain size of a selective tungsten film reduces reflectance and thereby enhances the ability of photolithography tools to focus and resolve photoresist images. However, the tungsten layer formed using the low temperatures described by Ahn et al. would be silicon rich (e.g., 3-4%) and would not be a good diffusion barrier for copper since copper resistivity would be degraded by the formation of copper silicide. Thus, it is difficult to deposit a diffusion barrier by selective means at low temperature. Moreover, the Ahn et al. technique relies on the formation of a donut shape at the bottom of the lines which is normally created by the reaction of outgassing moisture and WF_6. The creation of the donut shape is believed to be not reliable.

Dalton et al., VMIC Conference, June 12-13, 1990, pages 289-292, points out that a hot wall CVD reaction involving SiH_4 and H_2 reduction of WF_6 to form a selective tungsten layer on an aluminum or alloy conductor results in the incorporation of fluorine at the aluminum and tungsten interface. The fluorine incorporation is a byproduct of the reaction of WF_6 with aluminum as shown by Equation 1.

Eq. 1 $\quad WF_6 + 2Al \rightarrow 2AlF_3 + W$

The thin layer of aluminum fluoride will increase the series contact resistance of Metal 1 to Metal 2 vias. Dalton reported that sputtering TiW film on top of the aluminum prior to tungsten encapsulation using CVD eliminates the problem of fluorine absorption.

Dalton discloses a traditional scheme for interconnect formation wherein aluminum is first deposited on a planar surface, it is overcoated with the sputtered TiW layer (the only difference from traditional processing), the aluminum is then patterned using photoresist imaging and developing followed by reactive ion etching (RIE). The resulting structure is then overcoated with a passivation dielectric such as SiO_2 or polyimide which itself is subsequently patterned, subjected to RIE, and metallized to create a multilayered structure. Figure 1 is taken from Dalton and shows that multilayer devices produced by traditional processing schemes have seams in the dielectric layers at the location of the metal conductor lines and have a very irregular top surface.

It is difficult to achieve planarity of the dielectric using RIE. Planarity is in part dependent on the pattern density, and non-planar surfaces result in puddling problems during subsequent metallization. If an RIE technique is used on polyimide, an etch stop is needed for removal of photoresist on top of aluminum or copper based lines when the lines are etched down to the polyimide surface because the photoresist removal process would also remove polyimide. RIE of any high copper content, aluminum or copper alloy is extremely difficult. A serious drawback of traditional processes which include metal RIE is that a large number of metal shorts tend to develop with fine geometry due to particle defects.

U.S. Patent 4,824,802 to Brown et al. discloses a method for filling interlevel dielectric vias or contact holes in multilevel VLSI metallization structures. In particular, an intermediary metal such as tungsten or molybdenum is either selectively

deposited in openings in an insulator or non-selectively deposited over the entire surface and in the openings of the insulator by CVD, then a planarization resist, such as azoquinonenovolac-type resists, polymethacrylates, polyimides, or other thermoplastic materials, is applied over the top of the intermediary metal. A planarized structure is then obtained by etching to a level where the intermediary metal is even with the resist. The Brown et al. method does not avoid metal corrosion and other problems associated with etching and is not useful for planarizing Al-Cu or other soft alloys because they have different properties from the harder metals such as tungsten and molybdenum. Moreover, using the Brown et al. method, it is difficult to completely fill vias and lines.

U.S. Patent 4,944,836 to Beyer et al. discloses a chemical-mechanical polishing technique which can be used to produce coplanar metal/insulator films on a substrate. In particular, Beyer et al. contemplate patterning an underlying insulating layer, depositing an Al-Cu film, and then using a chemical-mechanical polishing technique wherein an alumina slurry in dilute nitric acid is mechanically rubbed on the surface to remove Al-Cu. The polishing compound tends to have a significantly higher removal rate for Al-Cu than the underlying insulator. The resulting structure includes Al-Cu lines planarized with the insulating layer, and subsequent layers can easily be added in the fabrication of multilayer structures.

U.S. Patent 4,956,313 to Cote et al. discloses a via filling and planarization technique wherein Al-Cu alloy lines are patterned on top of a first passivation layer on a substrate, the lines are overcoated with a second

passivation layer which is preferably a doped glass such as phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG) which conforms over the contours of the Al-Cu alloy lines, vias are then formed in the second passivation layer to expose the lines, and tungsten is applied over the surface of the second passivation layer and in the vias by CVD. It is reported in Cote et al. that CVD tungsten is conformal in character and can fill the vias without creating voids. The structure is then planarized by polishing with an abrasive slurry.

Neither Beyer et al. nor Cote et al. recognize that polishing is not practical for low resistivity, soft metals such as Al-Cu alloys. This is because such materials tend to scratch, smear on the surface, and corrode under the influence of the slurry. Moreover, creation of the planarized structures in accordance with Cote et al. takes several processing steps which increases costs and reduces output.

Rossnagel et al. J. Vac. Sci. Technol. 2:261 (Mar/Apr. 1991) discloses a collimated magnetron sputter deposition technique for depositing films that are compatible with lift-off patterning techniques and hole filling. The technique is also presented in U.S. Patent 4,824,544 which is herein incorporated by reference.

Shiozaki et al., Abstracts of the 19th Conference on Solid State Devices and Materials, discloses the use of selective tungsten deposition for hole filling on top of a high resistivity hard metal such as $MoSi_x$ and is unrelated to encapsulation of a soft metal.

SUMMARY OF THE INVENTION

It is an object of the present invention to ameliorate one or more disadvantages of the prior art.

According to one aspect of the present invention there is disclosed a method of creating a liner in high aspect ratio, submicron holes and lines comprising the step of sputtering a refractory metal or alloy through a collimator into a high aspect ratio, submicron hole or line in a dielectric at a pressure where scattering deposition dominates to create a conformal coating that is a liner.

According to another aspect of the present invention there is disclosed a method of forming a liner in high aspect ratio, submicron holes and lines, comprising the steps of: sputtering a refractory metal or alloy through a collimator into a high aspect ratio, submicron hole or line in a dielectric at a pressure where directional deposition dominates to create a conformal first layer in said high aspect ratio, submicron hole or line; and sputtering a refractory metal or alloy through a collimator into said high aspect ratio, submicron hole or line in said dielectric over said first layer at a pressure where scattering deposition dominates.

According to still another aspect of the present invention there is disclosed a method of creating metalization lines and vias on a substrate, comprising the steps of: forming an opening in a dielectric positioned on a substrate, said opening having a top and a bottom; depositing a first refractory metal or alloy or compound on a top surface of said dielectric and at a bottom of said opening; depositing a low resistivity metal or alloy over said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening to a point below said top of said opening; depositing a second refractory metal or alloy over said low resistivity metal or alloy on said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening; and removing said first refractory metal or alloy or compound, said low resistivity metal or alloy and said second refractory metal or alloy from all points above said top of said dielectric, whereby a planar structure is produced which includes a metalization site

having a low resistivity metal or alloy capped by a refractory metal or alloy that is planarized with said dielectric, said refractory metal or alloy being applied to said low resistivity metal or alloy at a temperature such that said low resistivity metal or alloy is unmelted, said low resistivity metal or alloy in said opening being encapsulated and wherein a liner is produced conforming to side walls of said opening.

According to still another aspect of the present invention there is disclosed a method of creating metalization lines and vias on a substrate, comprising the steps of: forming an opening in a dielectric positioned on a substrate, said opening having a top and a bottom; depositing a first refractory metal or alloy or compound on a top surface of said dielectric and at a bottom of said opening; depositing a low resistivity metal or alloy over said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening to a point below said top of said opening; depositing a second refractory metal or alloy over said low resistivity metal or alloy on said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening; and removing said first refractory metal or alloy or compound, said low resistivity metal or alloy, and said second refractory metal or alloy from all points above said top of said dielectric, whereby a planar structure is produced which includes a metalization site having a low resistivity metal or alloy capped by a refractory metal or alloy that is planarized with said dielectric, said refractory metal or alloy being applied to said low resistivity metal or alloy at a temperature such that said low resistivity metal or alloy is unmelted, wherein said step of depositing said first refractory metal or alloy or compound is achieved using collimated sputtering and a liner is produced which conforms to all inside surfaces of said opening and said top surface of said dielectric.

According to still another aspect of the present invention there is disclosed a method of creating metalization lines and vias on a substrate, comprising the steps of: forming an opening in a dielectric positioned on substrate, said opening having a top and

a bottom; depositing a first refractory metal or alloy or compound on a top surface of said dielectric and at a bottom of said opening; depositing a low resistivity metal or alloy over said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening to point below said top of said opening; depositing a second refractory metal or alloy over said low resistivity metal or alloy on said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening; and removing said first refractory metal or alloy or compound, said low resistivity metal or alloy, and said second refractory metal or alloy from all points above said top of said dielectric, whereby a planar structure is produced which includes a metalization site having a low resistivity metal or alloy capped by a refractory metal or alloy that is planarized with said dielectric, said refractory metal or alloy being applied to said low resistivity metal or alloy at a temperature such that said low resistivity metal or alloy is unmelted, wherein said step of depositing said first refractory metal or alloy is achieved using evaporation, whereby said refractory metal coats only said bottom of said opening but not side walls of said opening.

According to still another aspect of the present invention there is disclosed a method of creating metalization lines and vias on a substrate, comprising the steps of: forming an opening in a dielectric positioned on substrate, said opening having a top and a bottom; depositing a first refractory metal or alloy or compound on a top surface of said dielectric and at a bottom of said opening; depositing a low resistivity metal or alloy over said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening to point below said top of said opening; depositing a second refractory metal or alloy over said low resistivity metal or alloy on said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening; and removing said first refractory metal or alloy or compound, said low resistivity metal or alloy, and said second refractory metal or alloy from all points above said top of said dielectric, whereby a planar structure is produced which includes a metalization site having a low resistivity metal or alloy capped by a refractory metal or alloy that is

planarized with said dielectric, said refractory metal or alloy being applied to said low resistivity metal or alloy at a temperature such that said low resistivity metal or alloy is unmelted, wherein said step of removing said first refractory metal or alloy or compound, said low resistivity metal or alloy and said second refractory metal or alloy includes the step of reactive ion etching material above a top surface of said dielectric.

According to still another aspect of the present invention there is disclosed a method of creating metalization lines and vias on a substrate, comprising the steps of: forming an opening in a dielectric positioned on a substrate, said opening having a top and a bottom; depositing a first refractory metal or alloy or compound on a top surface of said dielectric and at a bottom of said opening; depositing a low resistivity metal or alloy over said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening to a point below said top of said opening; depositing a second refractory metal or alloy over said low resistivity metal or alloy on said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening; and removing said first refractory metal or alloy or compound, said low resistivity metal or alloy, and said second refractory metal or alloy from all points above said top of said dielectric, whereby a planar structure is produced which includes a metalization site having a low resistivity metal or alloy capped by a refractory metal or alloy that is planarized with said dielectric, said refractory metal or alloy being applied to said low resistivity metal or alloy at a temperature such that said low resistivity metal or alloy is unmelted, wherein said step of removing said first refractory metal or alloy or compound, said low resistivity metal or alloy and said second refractory metal or alloy includes the step of chemical-mechanical polishing material above a top surface of said dielectric.

According to still another aspect of the present invention there is disclosed a method of creating metalization lines and vias on a substrate, comprising the steps of: forming an opening in a dielectric positioned on a substrate, said opening having a top and a bottom; depositing a first refractory metal or alloy or compound on a top surface

of said dielectric and at a bottom of said opening; depositing a low resistivity metal or alloy over said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening to a point below said top of said opening; depositing a second refractory metal or alloy over said low resistivity metal or alloy on said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening; and removing said first refractory metal or alloy or compound, said low resistivity metal or alloy, and said second refractory metal or alloy from all points above said top of said dielectric, whereby a planar structure is produced which includes a metalization site having a low resistivity metal or alloy capped by a refractory metal or alloy that is planarized with said dielectric, said refractory metal or alloy being applied to said low resistivity metal or alloy at a temperature such that said low resistivity metal or alloy is unmelted, wherein said step of removing said first refractory metal or alloy or compound, said low resistivity metal or alloy and said second refractory metal or alloy includes both the steps of reactive ion etching and chemical-mechanical polishing material above a top surface of said dielectric.

According to still another aspect of the present invention there is disclosed a method of creating metalization lines and vias on a substrate, comprising the steps of: forming an opening in a dielectric positioned on substrate, said opening having a top and a bottom; depositing a first refractory metal or alloy or compound on a top surface of said dielectric and at a bottom of said opening; depositing a low resistivity metal or alloy over said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening to a point below said top of said opening; depositing a second refractory metal or alloy over said low resistivity metal or alloy on said refractory metal or alloy on said top surface of said dielectric and at said bottom of said opening; and removing said first refractory metal or alloy or compound, said low resistivity metal or alloy, and said second refractory metal or alloy from all points above said top of said dielectric, whereby a planar structure is produced which includes a metalization site having a low resistivity metal or alloy capped by a refractory metal or alloy that is

planarized with said dielectric, said refractory metal or alloy being applied to said low resistivity metal or alloy at a temperature such that said low resistivity metal or alloy is unmelted, wherein said step of removing said first refractory metal or alloy or compound, said low resistivity metal or alloy and said second refractory metal or alloy includes the step of wet etching with hydrogen peroxide or hydrogen tetraoxide.

According to still another aspect of the present invention there is disclosed a method of forming metalization lines and vias on a substrate, comprising the steps of: forming an opening in a dielectric positioned on a substrate, said opening having a top and a bottom; depositing a first metal or alloy or compound on a top surface of said dielectric and at a bottom of said opening; depositing a second metal or alloy over said first metal or alloy on said top surface of said dielectric and at said bottom of said opening to a point below said top of said opening; depositing a third metal or alloy over said second metal or alloy on said first metal or alloy or compound on said top surface of said dielectric and at said bottom of said opening, said third metal or alloy being relatively harder than said second metal or alloy; and removing said first metal or alloy or compound, said second metal or alloy, and said third metal or alloy from all points above said top of said dielectric, whereby a planar structure is produced which includes a metalization site having a second metal or alloy capped by a third metal or alloy, having a thickness so as to minimize a capacitance of the third metal or alloy, that is relatively harder than said second metal or alloy and is planarized with said dielectric, wherein said second metal or alloy is a metal having a resistivity lower than that of said third metal and said third metal is a refractory metal and wherein said third metal is deposited on said second metal at a temperature such that said second metal is unmelted.

According to yet another aspect of the present invention there is disclosed a method of creating a liner in high aspect ratio, submicron holes and lines comprising the step of sputtering a metal or alloy into a high aspect ratio, submicron hole or line in a dielectric at a pressure where directional deposition dominates, without collimation, to create a conformal coating that is a liner.

According to yet another aspect of the present invention there is disclosed a method of forming micron and sub-micron metalization lines and vias on a substrate, comprising the steps of: forming a micron or sub-micron sized opening in a dielectric positioned on a substrate, said opening having a top and a bottom; and filling said opening with a metal or metal alloy by sputtering said metal or metal alloy at a pressure below 1 mTorr without collimation into said micron or sub-micron sized opening, said metal or metal alloy uniformly filling said micron or sub-micron sized opening from said bottom towards said top to form a conformal coating thereover.

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a cross-sectional side view of a prior art semiconductor substrate showing an uneven top surface;

Figures 2A through 2E are sequential cross-sectional side views of a semiconductor substrate illustrating one variation of the invention;

Figures 3A and 3B are sequential cross-sectional side views of a substrate with a device thereon overcoated by an insulator being planarized prior to patterning the insulator;

Figures 4A through 4E are sequential cross-sectional side views of a semiconductor substrate illustrating another variation of the invention;

Figure 5A through 5E are sequential cross-sectional side views of a semiconductor substrate illustrating still another variation of the invention;

Figure 6 is a scanning electron micrograph (SEM) of a liner deposited in a via using PVD;

Figures 7A and 7B are sequential cross-sectional side views of a semiconductor substrate illustrating yet another variation of the invention;

Figure 8 is a cross-sectional view of an exemplary, multilevel, damascene structure wherein PVD Al_xCu_y alloy is capped with CVD tungsten; and

Figures 9A and 9B are cross-sectional SEM micrographs of structures with tungsten capped Al-Cu alloy lines prior to and after chemical-mechanical polishing, respectively.

The invention is generally related to methods for forming metal filled vias and conductor lines on a substrate where the vias and conductor lines include a soft, low resistivity metal which is capped with a relatively hard, refractory metal which is resistant to corrosion, wear, and electromigration, and where the vias and conductor lines are planar with a dielectric layer coated on the substrate. Several different and novel structures are created according to the procedures described in conjunction with Figures 2A-E, Figures 4A-E, and Figures 7A-B, depending on the PVD deposition technique utilized. It should be understood that the techniques and resulting structures are not limited to using any specific substrates and dielectric overlays (e.g., composites of inorganic and organic layers like that shown in Figures 2A-E and 5A-E can be used as well as single layers of inorganic or organic insulator materials). Moreover, the invention is not restricted to any particular metal combinations; rather, an objective of the invention is to overlay a soft, low resistance metal or metal alloy with a hard refractory metal which can withstand wear, corrosion and electromigration. The invention has particular relevance to electrical systems which use aluminum and copper alloys since it has been discovered that uniform, conformal coatings of a refractory metal liner material can be deposited in submicron vias and

trenches with reliable high aspect ratio filling using PVD collimated sputtering. The refractory metal liner will serve as an effective diffusion barrier to copper for subsequent processing.

With reference to Figure 2A, a substrate 10 is first overcoated with a dielectric which is subsequently patterned. The substrate 10 is preferably silicon, gallium arsenide, or some other material which is suitable for making integrated circuits. However, the substrate 10 may be a ceramic, glass, or composite material commonly used for packaging semiconductors and for making thin film interconnections. The substrate 10 preferably has a plurality of semiconductor devices formed therein which may include field effect transistors (FETs), bipolar transistors, resistors, Schottky diodes, or the like. It should be understood that the substrate 10 shown in each of Figures 3A-B, 4A-E, 5A-E, 7A-B, and 8, can have any of the attributes discussed above plus many other attributes known within the art.

The dielectric composite shown in Figure 2A includes top and bottom inorganic dielectric layers 11 and 13, respectively, which may be silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or the like. The inorganic layers 11 and 13 are both preferably deposited using plasma enhanced chemical vapor deposition (PECVD) where SiO_2 is first deposited at 90 Torr on the conducting substrate 10 and Si_3N_4 (0.075 to 0.1 μm) is provided as a barrier against mobile ion diffusion. A thicker organic dielectric layer 12, such as a polyimide, is deposited between the inorganic layers 11 and 13. Alternative to the dielectric composite created by layers 11, 12, and 13, a single layer of an inorganic dielectric, such as SiO_2, PSG, or BPSG, or an organic

dielectric, such as polyimide, may also be employed and may be deposited by any of a number of well known techniques such as by growing in an oxidative atmosphere, sputtering, or PECVD. While Figures 2A-E and 5A-E show the use of the composite structure and Figures 3A-B, 4A-E, and 7A-B show the use of a single inorganic or dielectric layer, it should be understood that the dielectric layer is not limiting to the practice of this invention and that any dielectric (e.g., inorganic or organic) used by itself or in combination could be employed in the practice of this invention.

Figure 2A shows an opening 14 formed in the dielectric composite, and this opening may be a via or a trench for a conductive line. In VLSI applications, the substrate 10 is likely to have several hundred to thousands of openings 14 like that shown in Figure 2A where the resulting dense, complex pattern will ultimately interconnect circuits on or in the substrate. The openings 14 are preferably formed using contrast enhanced lithography (CEL) followed by trench or hole etching with a multiwafer tool using CHF_3 and O_2 with an optimum overetch to ensure that the opening 14 has the desired dimensions and extends to a contact on the surface of the substrate 10 for a via stud pattern. For line patterns, the dielectric layers are preferably partially etched to a depth about 10% higher than the metal thickness to be employed. When etching polyimide 12, O_2 RIE at low temperatures is preferred. It should be understood that the formation of the opening 14, as indicated in Figures 2A-E, 4A-E, 5A-E, and 7A-B, is well understood within the art and can be created by many different techniques.

If the starting substrate 10 has a device 18 formed thereon as is shown in Figures 3A and 3B, as opposed to the flat substrate 10 with no upwardly protruding devices as is shown in Figure 2A, the insulator 20 coated over the device 18 should first be planarized before an opening 22 is created. Planarization can be achieved by RIE, chemical-mechanical polishing, a combination of both RIE and chemical-mechanical polishing, or by other means.

Figures 2B-2E illustrate a first variation of the present invention wherein a planar patterned structure, which can be either the one shown in Figure 2A or the one shown in Figure 3B or any other structure which has an opening 14 formed in an overcoated dielectric, then has a refractory metal layer 15 deposited over the inorganic dielectric layer 13 and on the exposed substrate 10 at the bottom of gap 14. This is accomplished using an evaporation PVD technique best described in Handbook of Thin Film Technology, eds. Maissel and Glen, McGraw-Hill Co., 1983, pp. 1-100. An important feature of employing evaporation PVD at this point is that the refractory metal layer 15 does not coat the side walls of the opening 14 in the dielectric. It should be understood that PVD collimated sputtering, similar to that described in U.S. Patent 4,824,544, can be used in the practice of the invention, but that collimated sputtering produces a conformal layer which would coat the side walls of opening 14, contrary to that which is shown in Figure 2B. The use of collimated sputtering to create a refractory metal liner is discussed in more detail below. The refractory metal may be titanium (Ti), titanium alloys or compounds such as Ti/TiN, tungsten (W), titanium/tungsten (Ti/W) alloys, or chromium (Cr) or tantalum (Ta) and their alloys, or some other

suitable material. If copper based lines or vias are to be formed, a refractory metal should be used which can act as a diffusion barrier to copper such that diffusion during subsequent processing of deposited copper in the opening 14 into the substrate 10 is prevented.

Next, a single, binary or ternary metallization 16 is deposited over the refractory metal 15 by PVD using evaporation. Again, since evaporation is used, the side walls of opening 14 are not coated. However, it should be understood that the metallization 16 could be applied by collimated sputtering, in which case a conformal coating of the metallization within the opening 14 and on top of the dielectric stack. Preferably, the metallization is Al_xCu_y, where the sum of x and y is equal to one and both x and y are greater than or equal to zero and less than or equal to one; however, ternary alloys such as Al-Pd-Cu and multicomponent alloys such as Al-Pd-Nb-Au would also be suitable. The principle characteristic of the metallization 16 is that it is a low resistivity and soft material compared to the refractory metal 15. Preferably, the opening 14, which represents the line pattern or interlevel via pattern, is filled with the metallization 16 to a depth of 100 to 400 nm below the surface of the line or via. It should be understood that the metallization 16 shown in Figures 4A-E, 5A-E, and 7A-B would be of the same sort described above.

Figure 2C shows a refractory metal 17, such as tungsten, cobalt, nickel, molybdenum, or alloys/compounds such as Ti/TiN, deposited over the structure. Deposition of the refractory metal 17 may be by one step CVD or by a two step process, as is best explained in Figures 4a-e, wherein the first step

involves collimated sputtering or the like of an adhesion promoting compound such as titanium or titanium nitride to create a conformal blanket coating, and the second step includes depositing a thin CVD layer of tungsten to achieve a higher degree of conformality. CVD deposition of the refractory metal is preferably achieved with SiH_4 or H_2 reduction of WF_6. A particularly preferred CVD procedure involves SiH_4 reduction of WF_6 followed by H_2 reduction of WF_6 because, on top of a TiN layer, CVD of tungsten proceeds smoothly with SiH_4 reduction of WF_6, but not with H_2 reduction. The refractory metal 17 provides a wear resistant, corrosion resistant, and electromigration resistant coating to the underlying soft, low resistivity metallization 16 in opening 14. A particularly good advantage to using CVD with SiH_4 reduction of WF_6 is that the ratio of SiH_4 to WF_6 can be varied to incorporate different amounts of silicon into the tungsten to achieve beneficial properties. For example, it would be preferable to deposit the refractory metal 17 at a 0.5 SiH_4 to WF_6 ratio while the opening 14 in the dielectric is being filled since so doing will result in a lower resistance refractory metal; however, towards the top surface of the dielectric to deposit at a 2.0 SiH_4 to WF_6 ratio since this will result in more silicon incorporation which has greater wear resistance. Using the above-described CVD technique, the silicon doped tungsten can be used as a wear resistant coating or a polishing stop (e.g., it will be more resistant to an alumina slurry in ferric nitrate used in chemical-mechanical polishing). Because the metallization 16 applied by evaporation does not coat the side walls of the opening 14, the CVD applied refractory metal 17 creates tapering side walls around the metallization 16 and the metallization 16 becomes completely encapsulated in refractory metal 17 and underlying refractory metal 15.

Figures 2D and 2E show that structure is planarized after the CVD application of the refractory metal 17 to yield a structure wherein a two part conductive via or line, which includes a central, soft, low resistivity metallization 16, encapsulated in a hard, wear resistant refractory metal 17, has a top surface which is even with the top surface of the dielectric composite on substrate 10. Planarization can be accomplished within one or two steps by chemical-mechanical polishing with a slurry such as alumina in dilute ferric nitrate or by RIE in the presence of SF_6 or Cl_2 based chemistry. If chemical-mechanical polishing is employed, slurries can be selected to remove different metal layers on the stack. For example, Ti/TiN/W on top of copper can be removed using the alumina in dilute ferric nitrate slurry, and then the remaining copper can be removed by switching to a slurry without alumina. Combinations of RIE removal of the refractory metal layer 17 followed by chemical-mechanical polishing of the remaining metallization 16 and remaining refractory metal 17 above the top organic or inorganic layer 13 are also contemplated. A particular planarization procedure contemplated includes removing tungsten refractory metal 17 by either chemical-mechanical polishing or RIE with SF_6 or Cl_2 based chemistry down to an Al-Cu alloy metallization 16 surface as shown in Figure 2D, then, using the tungsten as a mask, the Al-Cu CVD layer is etched down to the inorganic layer 13 surface, and finally, the remaining tungsten 17 on the dielectric surface is either polished, wet etched or RIE etched in Cl_2 to yield the structure shown in Figure 2E.

Figures 4A through 4E show another variation on the invention where like elements to those identified above are indicated by the same numerals in each of the

Figures. As shown in Figure 4A, copper metallization 16 is deposited in an opening 14 created in an inorganic or organic dielectric 15 formed on substrate 10. The chief difference between the structure shown in Figure 4A and the structure shown in Figure 2B is that prior to deposition of copper metallization, a thin layer of refractory metal 24 such as titanium, titanium nitride (TiN), tungsten, tantalum, or alloys and compounds thereof, is deposited over the inorganic or organic dielectric 15 surface and inside the opening 14 via collimated sputtering.

As noted above, collimated sputtering is generally described in U.S. Patent 4,824,544 to Rossnagel et al. where a lift-off procedure is discussed. In the present invention, it has been discovered that employing collimated sputtering at higher pressures where scattering dominates, as opposed to lower pressures where directional deposition dominates, allows for the creation of conformal coatings within a high aspect ratio, submicron level trench or via (e.g., both the side walls and base are coated). The aspect ratio generally refers to the ratio of the height of a trench or via relative to its width in the case of a trench or its diameter in the case of a via. Trenches and vias with aspect ratios greater than two are generally considered to have a high aspect ratio. With collimated sputtering, scattering tends to dominate above pressures of 1mTorr (preferably around 3mTorr), while directional deposition dominates below 1mTorr. Collimated sputtering is described in more detail below in conjunction with Figures 5A-E and 6.

Completely coating the bottom surface and side walls of opening 14 with a refractory metal layer 24, as shown in Figure 4a, is especially important when a copper

based alloy metallization 16 is used since copper will diffuse into the substrate 10 during subsequent high temperature processing and ruin the device if no diffusion barrier is provided. The copper metallization 16 can be deposited by PVD using either evaporation or collimated sputtering or by other techniques. When submicron, high aspect ratio holes are to be filled, prior art CVD techniques have been unsuccessful for filling the holes with aluminum and copper based alloys; therefore, the preferred method for filling is by PVD techniques.

Subsequent to deposition of metallization 16, a thin layer 26 of titanium, Ti/TiN, tantalum or chromium is then applied over the copper metallization 16 surface to promote adhesion. A refractory metal such as tungsten is then deposited by CVD by SiH_4 or H_2 reduction of WF_6 to yield the structure shown in Figure 4B. As explained above, varying the SiH_4 to WF_6 ratio during CVD can advantageously be used to make a harder, more wear resistant, tungsten with incorporated silicon layer near the top surface of the dielectric 15. The interfacial thin layer 26 should be chosen so that it does not attack the underlying copper metallization 16.

Figure 4c shows that first tungsten is planarized by polishing or by RIE and Figure 4d shows that copper is selectively removed by wet etching. When copper or copper alloy lines are being created, it is advantageous to use a wet etch solution based on hydrogen peroxide (H_2O_2) and hydrogen tetroxide (H_2O_4) to planarize the copper. At room temperature, this type of solution will not etch tungsten or dielectric, but will etch off all copper positioned above the dielectric since it is not protected from the wet etch solution (e.g., at room temperature, H_2O_2 has almost

infinite selectivity). Figure 4e shows that after the wet etch, the tungsten 17 can be selectively removed by RIE, polishing or other techniques. A preferred method for removing the tungsten refractory metal 17 which projects above the dielectric 15 surface is by chemical-mechanical polishing using an alumina in ferric nitrate slurry or the like. Because tungsten is a relatively hard material, it does not scratch or corrode when subjected to chemical-mechanical polishing. Rather than the three step approach discussed above, it may be preferable to remove the tungsten refractory metal 17, the thin layer 26 adhesion promoter, and the copper metallization 16 located above the surface of the insulator 15 in one step using chemical-mechanical polishing.

Figures 5A through 5E show yet another variation on the invention where like numerals indicate like elements. Figure 5A shows a refractory metal liner 28 is deposited in the opening 14 prior to metallization in a fully or partially conformal manner using collimated sputtering like that described in Rossnagel et al. J. Vac. Sci. Technol. 2:261 (Mar/Apr. 1991) and U.S. Patent 4,824,544 to Rossnagel et al. which are herein incorporated by reference. In collimated sputtering, refractory metal atoms are passed through a honeycomb like structure with an aspect ratio of depth to area of greater than one at pressures greater than 0.5 mTorr. Table 1 presents conditions which have been used for liner deposition.

TABLE 1

DEPOSITION OF LINER BY COLLIMATION

ASPECT RATIO	STEP COVERAGE SIDEWALL/TOP (%)	BOTTOM/TOP (%)
1:1	38	60
1:2	39	70
1:4	42	100
NO COLLIMATION		
0	10	12

In the investigations presented in Table 1, the pressure was varied from 0.5mT to 15 mT and the power was varied from 0.5 kW to 12 kW. Table 1 clearly indicates poor step coverage when collimation is not employed. Using higher pressures (e.g., 3 mTorr) and a collimator with aspect ratios of at least 1:1, the vias or contacts with aspect ratios of more 7 to 8 were coated with Ti/TiN or Ti/W bilayers resulting in step coverage more than 40% at the bottom and more than 30% on the side wall. This is a significant advance in the art since it allows semiconductor manufacturers to provide a conformal layer within a high aspect ratio trench or via which will promote adhesion of CVD tungsten. Moreover, as will be discussed in more detail below, providing a conformal layer of TiN or other suitable materials will provide an effective diffusion barrier for copper based alloys. As discussed above, in order to thoroughly coat the side walls and bottom of a trench or via pressures should be employed where scattering deposition dominates (e.g., above 1 mTorr) rather than at lower pressures where directional deposition dominates.

Figure 6 presents an SEM micrograph of a refractory metal liner in a via created by PVD collimated sputtering as described above. Figure 6 shows that complete coverage of the bottom and sidewalls of the

via can be obtained. To deposit TiN in-situ, N_2 plasma was used along with argon in the presence of a titanium target. The liner can improve adhesion and prevent any attack of CVD tungsten on the underlying substrate. The conformality of a liner increase when the aspect ratio of the collimator increases.

When copper lines or vias are to be employed in the structure, a robust liner which can serve as a diffusion barrier is required. Low pressure collimation of a refractory liner (e.g., Ta, Ti/TiN, or Ti/W, etc.) created a porous structure on the side wall of the opening 14 in the dielectric. To prevent this porous structure and provide a dense structure on the side wall, a two step collimation process was employed. Specifically, in the first step, a thin liner was deposited using a pressure below 0.8 mT to get bottom coverage of more than 60%, and in the second step, the pressure was increased in-situ to 3 to 4 mT to get a dense microstructure on the sidewall using the same collimator. Prior to this invention, there was no means available for forming a liner in high aspect ratio, submicron holes, especially at low temperatures. The results were similar for Ti/W and Ti/TiN bilayer liners used as a diffusion barrier for CVD refractory metal 17 or low resistivity soft metal.

Figures 5B-E show similar steps to those shown in Figures 2B-E and Figures 4A-E are performed in another variation on the invention. Like in Figure 4A, Figure 5B shows that an adhesion promoter layer 26, such as Ti, Cr, Ta, Ti/W, or the like, is deposited by PVD evaporation over the top of the refractory metal liner and in the bottom of the gap 14. Like in Figure 2B, Figure 5B shows Al-Cu alloy or other metallization 16 being deposited by PVD evaporation techniques to a

level 100 to 400 nm below the surface of the dielectric. Figures 5C-E respectively show deposition of a conformal layer of tungsten or other refractory material to cap the low resistivity metallization 16, planarizing the tungsten by RIE or polishing, or the like, and planarizing the structure using the two step wet etching of the aluminum-copper alloy with H_2O_2 followed by chemical-mechanical polishing of tungsten as shown in Figures 4c and 4d or simply planarizing by one step RIE or chemical-mechanical polishing. For one step chemical-mechanical polishing, a slurry similar to that used for tungsten polishing can be used. Like the structure shown in Figure 2E, the structure shown in Figure 5E has a CVD refractory metal 17 encapsulating a low resistivity metallization 16 where there is a tapered refractory metal 17 region.

Figures 7A and 7B show yet another variation on the invention where like elements are indicated by like numerals. As shown in Figure 7A, both a conformal, preferably refractory metal, liner/diffusion barrier 28 and a conformal Al_xCu_y or other suitable, low resistivity alloy or metallization 16 layer are deposited in the opening in the organic or inorganic dielectric 15 on substrate 10 using PVD collimated sputtering procedures. Subsequently, a refractory metal 17 capping layer, such as tungsten, titanium, tantalum, or the like, is deposited by CVD to blanket coat the structure. Figure 7B shows that the structure is then planarized using RIE, chemical-mechanical polishing, or by other techniques. Contrasting the structure of Figure 7B with the structure of Figure 5E, it can be seen that the shape of the via or line is quite different. While both structures include a low resistivity metal 16 capped by a refractory metal 17, the two metallizations will likely serve different environments.

Experimental tests have been conducted with the refractory metal capped lines fabricated according to the techniques discussed above. In the experiments, the line lengths varied from 13.5 cm to 50 cm with an area of the chip close to 1.6 mm^2. The metal pitches varied from 1μm to 2μm. The aspect ratio of the holes filled were from 2 to 8 and for lines 2 to 4. Table 2 presents the resistance test results.

TABLE 2

LINE RESISTANCE OF TUNGSTEN CAPPED LOW RESISTIVITY METAL AFTER POLISHING[a]

(A) CREATED USING EVAPORATION[b]

Structure	Resistance before W dep.	Resistance after W dep.	Yield
Ti(20nm)/TiN(35nm)/Al-Cu(800nm)/W(200nm)	0.042	0.04	95%
Ti(20nm)/Al-Cu(800nm)/W(200nm)	0.042	0.052	95%
Ti(20nm)/Al-Cu(800nm)/Ti(20nm)/W(200nm)	0.042	0.054	94%
Ti(20nm)/TiN(25nm)/CVD W(30nm)/Al-Cu(1300nm)/ W(200nm)	0.025	0.023	97%
Ti(50nm)/TiN(25nm)/Ti(20nm)/Al-Cu(1300nm)/Ti(20nm)/ TiN(20nm)/W(200nm)	0.025	0.032	96%
Ti(50nm)/TiN(50nm)/Ti(50nm)/Al-Cu(600nm)/Ti(20nm)/ Cu(700nm)/Ti(20nm)/TiN(20nm)/CVD W(200nm)	0.023	0.021	100%

(B) CREATED USING COLLIMATED SPUTTERING[c]

Ti(20nm)/TiN(35nm)/Al-Cu(800nm)/CVD W(200nm)			
	0.042	0.04	84%
Ti(20nm)/Al-Cu(800nm)/CVD W(200nm)			
	0.042	0.05	81%
Ti(20nm)/W(20nm)/Al-Cu(800nm)/CVD W(200nm)			
	0.040	0.039	85%
Ti(20nm)/TiN(75nm)/Cu(800nm)/Ti(20nm)/TiN(25nm)/CVD W(200nm)			
	0.024	0.022	80%

(C) CREATED USING SPUTTERING WITHOUT COLLIMATION[d]

Ti(20nm)/TiN(35nm)/Al-Cu(800nm)/CVD W(200nm)			
	0.040	0.04	86%

[a]In all the experiments, the line lengths varied from 13.5 to 50 cm with an are of the chip close to 1.6 mm^2. The metal pitches varied from 1μm to 2μm. The aspect ratio of the holes filled were from 2 to 8 and for lines, 2 to 4.

[b]In the Evaporation Experiments, Ti/TiN bilayers were deposited by collimation sputtering.

[c]Colimation aspect ratio of 1:1.

[d]Sputtering pressure ranged between 0.5 to 0.8mTorr.

The results in Table 2 show that the process yield for the new technique is very good and that the line resistance is not altered greatly by the presence of the tungsten cap. Some of the above data shows an increase in resistance when titanium is present directly under Al-Cu alloy. This is due to the formation of $TiAl_3$ at the interface. It has been found

that providing a titanium alloy or compound (e.g., TiN) between titanium and the aluminum-copper layer prevents the formation of $TiAl_3$ and thereby keeps the resistance lower. The bottom entry in Table 2 shows that if sputtering without collimation is employed, the sputtering should take place at lower pressures (e.g., below 1 mTorr) and be directionally dominated.

It is anticipated that performing RIE or a wet etch using H_2O_2 or H_2O_4 on the refractory metal cap after chemical-mechanical polishing will be advantageous in bringing the thickness of the capping layer down to a bare minimum. A thick layer of a refractory metal would increase capacitance, which is not desirable. By allowing for a post-polishing wet etch or RIE procedure (e.g, SF_6 etching), the semiconductor designer will be able to use thick layers of refractory metal to provide maximum protection for the underlying low resistivity Al-Cu line or via during chemical-mechanical polishing, yet will be able to subsequently remove any excess refractory metal to achieve a structure which has very little overlying refractory metal. For example, an 500-600nm thick refractory layer can be applied and used for protection against polishing damage, and then the refractory layer can be reduced down to a 50nm thick layer by wet etching or RIE.

Figure 8 shows an example of one multilevel semiconductor device which includes a top surface having tungsten capped Al_xCu_y alloy lines flush with the top most insulator layer. As discussed in detail above, the vias or trenches with CVD tungsten preferably include a TiN liner formed by collimated sputtering to promote adhesion. Many other semiconductor devices can be fabricated within the practice of this invention.

Figures 9a and 9b are SEM micrographs of a cross-section of a semiconductor device. Figure 9a shows separated SiO_2 portions projecting up from a silicon surface with Al-Cu alloy between and on top of the SiO_2. Between and on top of the Al-Cu alloy is a CVD tungsten layer. Figure 9a represents a structure with capped lines prior to polishing. Figure 9b shows an SEM micrograph of the cross-section of a multilayer structure after chemical-mechanical polishing has removed the tungsten and Al-Cu alloy above the top surface of the SiO_2 projections.

CLAIMS

The claims defining the invention are as follows:

1. A semiconductor device comprising:

a dielectric layer;

at least one high aspect ratio submicron hole or line in the dielectric layer,

the at least one hole or line having sidewalls and a bottom; and

a liner in the at least one hole or line, the thickness of the liner on the bottom being greater than the thickness of the liner on the sidewalls wherein said liner includes copper.

2. The semiconductor device of claim 1 wherein the copper or copper-containing alloy is defined as $Al_x Cu_y$ where x+y=1 and x and y are less than or equal to 1.

3. The semiconductor device of claim 1 wherein the liner is substantially conformal.

4. The semiconductor device of claim 1 wherein the liner comprises a a refractory metal.

5. The semiconductor device of claim 4 wherein the refractory metal included tantalum.

6. The semiconductor device of claim 1 wherein the aspect ratio of the hole or line is greater than about 2:1.

7. The semiconductor device of claim 1 wherein the ratio of the thickness of the liner on the bottom to the thickness of the liner on the sidewalls is at least about 4:3.

8. The semiconductor device of claim 1 wherein the ratio of the thickness of the liner on the bottom to the thickness of the liner on the sidewalls is at least about 1.5:1.

9. The semiconductor device of claim 1 wherein the liner includes two layers.

10. The semiconductor device of claim 9 wherein each layer of the liner comprises a refractory metal or an alloy or compound thereof.

11. The semiconductor device of claim 1 wherein the liner includes a sputter deposited refractory metal.

12. A semiconductor device comprising:

a dielectric layer;

at least one high aspect ration submicron hole or line in the dielectric layer, the at least one hole or line having sidewalls and a bottom; and

a liner in the at least one hole or line, the thickness of the liner on the bottom being greater than the thickness of the liner on the sidewalls, wherein said liner comprises a refractory metal including tantalum.

13. The semiconductor device of claim 12 wherein the aspect ratio of the hole or line is greater than about 2:1.

14. The semiconductor device of claim 12 wherein the ratio of the thickness of the liner on the bottom to the thickness of the liner on the sidewalls is at least about 4:3.

15. The semiconductor device of claim 12 wherein the ratio of the thickness of the liner on the bottom to the thickness of the liner on the sidewalls is at least about 1.5:1.

16. The semiconductor device of claim 12 wherein the liner includes a sputter deposited refractory metal.

17. A semiconductor device comprising:

a dielectric layer;

at least one high aspect ration submicron hole or line in the dielectric layer, the at least one hole or line having sidewalls and a bottom; and

a liner in the at least one hole or line, the thickness of the liner on the bottom being greater than the thickness of the liner on the sidewalls wherein said liner includes two layers.

18. The semiconductor device of claim 17 wherein each layer of the liner comprises a refractory metal.