Heating Plate with Planar Heater Zones for Semiconductor Processing

Background of the Disclosure

[0001] With each successive semiconductor technology generation, substrate diameters tend to increase and transistor sizes decrease, resulting in the need for an ever higher degree of accuracy and repeatability in substrate processing. Semiconductor substrate materials, such as silicon substrates, are processed by techniques which include the use of vacuum chambers. These techniques include non plasma applications such as electron beam deposition, as well as plasma applications, such as sputter deposition, plasma-enhanced chemical vapor deposition (PECVD), resist strip, and plasma etch.

[0002] Plasma processing systems available today are among those semiconductor fabrication tools which are subject to an increasing need for improved accuracy and repeatability. One metric for plasma processing systems is increased uniformity, which includes uniformity of process results on a semiconductor substrate surface as well as uniformity of process results of a succession of substrates processed with nominally the same input parameters. Continuous improvement of on-substrate uniformity is desirable. Among other things, this calls for plasma chambers with improved uniformity, consistency and self diagnostics.

Summary of the Invention

[0003] In accordance with one embodiment, a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor plasma processing apparatus, comprises at least a first electrically insulating layer, planar heater zones comprising at least first, second, third and fourth planar heater zones laterally distributed across the first electrically insulating layer, electrically conductive power supply lines comprising at least a first power supply line electrically connected to the first and second heater zones and a second power supply line electrically connected to the third and fourth heater zones, electrically conductive power return lines comprising at least a first power return line

electrically connected to the first and third heater zones, and a second power return line electrically connected to the second and fourth heater zones.

Brief Description of Drawings

[0004] **Fig. 1** is a schematic of the cross-sectional view of a substrate support assembly in which a heating plate with an array of heater zones is incorporated, the substrate support assembly also comprising an electrostatic chuck (ESC).

[0005] **Fig. 2** illustrates the topological connection between power supply and power return lines to an array of heater zones in one embodiment of a heating plate which can be incorporated in a substrate support assembly.

[0006] **Fig. 3A** shows an embodiment wherein the power supply lines and the heater zones are on the same plane.

[0007] **Fig. 3B** shows the power return lines on a plane separated from the plane in Fig. 3A by an electrically insulating layer and the power return lines are connected to the heater zones through vias extending through the electrically insulating layer.

[0008] **Fig. 3C** is a schematic of the cross-sectional view of a substrate support assembly in which the heating plate of Fig. 3A and 3B is incorporated.

[0009] **Fig. 4A** shows an embodiment wherein the power supply lines and the heater zones are on the same plane.

[0010] **Fig. 4B** shows a plane separated from the plane in Fig. 4A by an electrically insulating layer wherein the power supply lines are connected to leads in this plane through vias, and brought to a single hole in the cooling plate (not shown). The power return lines on this plane are connected to the heater zones through vias extending between this plane and the plane in Fig. 4A. The power return lines are also brought to a single hole in the cooling plate (not shown).

[0011] **Fig. 5A** shows an embodiment wherein the heater zones are on a plane without the power supply lines or power return lines on that plane. The heater zones are connected to power supply lines and power return lines on one or more different planes through vias.

[0012] **Fig. 5B** shows the power supply lines on a second plane separated from the plane in Fig. 5A by an electrically insulating layer. The power supply lines are

connected to the heater zones through vias extending between the two planes in Fig. 5A and 5B.

[0013] **Fig. 5C** shows the power return lines on a third plane separated from the planes in Fig. 5A and 5B by another electrically insulating layer. The power return lines are connected to the heater zones through vias extending between all three planes in Fig. 5A-C. The leads connected to the power supply lines in Fig. 5B are also routed through feedthroughs in this plane.

[0014] **Fig. 5D** is a schematic of the cross-sectional view of a substrate support assembly in which the heating plate in Fig. 5A-C is incorporated.

[0015] **Fig. 5E** is a schematic of the cross-sectional view of a substrate support assembly in which an alternative heating plate in Fig. 5A-C is incorporated.

[0016] **Fig. 6** is a schematic of the cross-sectional view of a substrate support assembly in which a heating plate is incorporated, the substrate support assembly further including a primary heater layer above the array of heater zones, the primary heater located on an additional plane separated from all the planes in the heating plate by an electrically insulating layer.

[0017] **Fig. 7A** is a schematic of an exemplary plasma processing chamber, which can include a substrate support assembly with the heating plate described herein.

[0018] **Fig. 7B** is a schematic of an RF isolation approach.

[0019] **Fig. 8** shows a block diagram of signal flow in one embodiment of the control electronics for the substrate support assembly.

Detailed Description

[0020] Radial and azimuthal substrate temperature control in a semiconductor processing apparatus to achieve desired critical dimension (CD) uniformity on the substrate is becoming more demanding. Even a small variation of temperature may affect CD to an unacceptable degree, especially as CD approaches sub-100nm in semiconductor fabrication processes.

[0021] A substrate support assembly may be configured for a variety of functions during processing, such as supporting the substrate, tuning the substrate temperature, and power supplying radio frequency power. The substrate support assembly can comprise an electrostatic chuck (ESC) useful for electrostatically clamping a

substrate onto the substrate support assembly during processing. The ESC may be a tunable ESC (T-ESC). A T-ESC is described in commonly assigned U.S. Patent Nos. 6,847,014 and 6,921,724, which are hereby incorporated by reference. The substrate support assembly may comprise a ceramic substrate holder, a fluid-cooled heat sink (hereafter referred to as cooling plate) and a plurality of concentric heater zones to realize step by step and radial temperature control. Typically, the cooling plate is maintained between 0 °C and 30 °C. The heaters are located on the cooling plate with a layer of thermal insulator in between. The heaters can maintain the support surface of the substrate support assembly at temperatures about 0 °C to 80 °C above the cooling plate temperature. By changing the heater power within the plurality of heater zones, the substrate support temperature profile can be changed between center hot, center cold, and uniform. Further, the mean substrate support temperature can be changed step by step within the operating range of 0 to 80 °C above the cooling plate temperature. A small azimuthal temperature variation poses increasingly greater challenges as CD decreases with the advance of semiconductor technology.

[0022] Controlling temperature is not an easy task for several reasons. First, many factors can affect heat transfer, such as the locations of heat sources and heat sinks, the movement, materials and shapes of the media. Second, heat transfer is a dynamic process. Unless the system in question is in heat equilibrium, heat transfer will occur and the temperature profile and heat transfer will change with time. Third, non-equilibrium phenomena, such as plasma, which of course is always present in plasma processing, make theoretical prediction of the heat transfer behavior of any practical plasma processing apparatus very difficult if not impossible.

[0023] The substrate temperature profile in a plasma processing apparatus is affected by many factors, such as the plasma density profile, the RF power profile and the detailed structure of the various heating the cooling elements in the chuck, hence the substrate temperature profile is often not uniform and difficult to control with a small number of heating or cooling elements. This deficiency translates to non-uniformity in the processing rate across the whole substrate and non-uniformity in the critical dimension of the device dies on the substrate.

[0024] In light of the complex nature of temperature control, it would be advantageous to incorporate multiple independently controllable heater zones in the substrate support assembly to enable the apparatus to actively create and maintain the desired spatial and temporal temperature profile, and to compensate for other adverse factors that affect CD uniformity.

[0025] Described herein is a heating plate for a substrate support assembly in a semiconductor processing apparatus with multiple independently controllable heater zones. This heating plate comprises a scalable multiplexing layout scheme of the heater zones and the power supply and power return lines. By tuning the power of the heater zones, the temperature profile during processing can be shaped both radially and azimuthally. Although this heating plate is primarily described for a plasma processing apparatus, this heating plate can also be used in other semiconductor processing apparatuses that do not use plasma.

[0026] Also described are methods for manufacturing this heating plate, a substrate support assembly comprising such a heating plate, and methods for powering and controlling a substrate support assembly comprising such a heating plate.

[0027] The heater zones in this heating plate are preferably arranged in a defined pattern, for example, a rectangular grid, a hexagonal grid, a polar array, concentric rings or any desired pattern. Each heater zone may be of any suitable size and may have one or more heater elements. All heater elements in a heater zone are turned on or off together. To minimize the number of electrical connections, power supply and power return lines are arranged such that each power supply line is connected to a different group of heater zones and each power return line is connected to a different group of heater zones with each heater zone being in one of the groups connected to a particular power supply line and one of the groups connected to a particular power return line. No two heater zones are connected to the same pair of power supply and power return lines. Thus, a heater zone can be activated by directing electrical current through a pair of power supply and power return lines to which this particular heater zone is connected. The power of the heater elements is preferably smaller than 20W, more preferably 5 to 10 W. The heater elements may be resistive heaters, such as polyimide heaters, silicone rubber heaters, mica heaters, metal heaters (e.g. W, Ni/Cr alloy, Mo or Ta), ceramic heaters (e.g. WC),

semiconductor heaters or carbon heaters. The heater elements may be screen printed, wire wound or etched foil heaters. In one embodiment, each heater zone is not larger than four device dies being manufactured on a semiconductor substrate, or not larger than two device dies being manufactured on a semiconductor substrate, or not larger than one device die being manufactured on a semiconductor substrate, or between 2 and 3 cm^2 in area to correspond to the device dies on the substrate. The thickness of the heater elements may range from 2 micrometers to 1 millimeter, preferably 5-80 micrometers. To allow space between heater zones and/or power supply and power return lines, the total area of the heater zones may be up to 90% of the area of the upper surface of the substrate support assembly, e.g. 50-90% of the area. The power supply lines or the power return lines (power lines, collectively) may be arranged in gaps ranging from 1 to 10 mm between the heater zones, or in separate planes separated from the heater zones plane by electrically insulating layers. The power supply lines and the power return lines are preferably made as wide as the space allows, in order to carry large current and reduce Joule heating. In one embodiment, in which the power lines are in the same plane as the heater zones, the width of the power lines is preferably between 0.3 mm and 2 mm. In another embodiment, in which the power lines are on different planes than the heater zones, the width of the power lines can be as large as the heater zones, e.g. for a 300 mm chuck, the width can be 1 to 2 inches. The materials of the power supply and power return lines may be the same as or different from the materials of the heater elements. Preferably, the materials of the power supply and power return lines are materials with low resistivity, such as Cu, Al, W, Inconel® or Mo.

[0028] Figs. 1-2 show a substrate support assembly comprising one embodiment of the heating plate having an array of heater zones **101** incorporated in two electrically insulating layers **104A** and **104B**. The electrically insulating layers may be a polymer material, an inorganic material, a ceramic such as silicon oxide, alumina, yttria, aluminum nitride or other suitable material. The substrate support assembly further comprises (a) an ESC having a ceramic layer **103** (electrostatic clamping layer) in which an electrode **102** (e.g. monopolar or bipolar) is embedded to electrostatically clamp a substrate to the surface of the ceramic layer **103** with a DC

voltage, (b) a thermal barrier layer **107**, (c) a cooling plate **105** containing channels **106** for coolant flow.

[0029] As shown in Fig. 2, each of the heater zones **101** is connected to one of the power supply lines **201** and one of the power return lines **202**. No two heater zones **101** share the same pair of power supply **201** and power return **202** lines. By suitable electrical switching arrangements, it is possible to connect a pair of power supply **201** and power return **202** lines to a power supply (not shown), whereby only the heater zone connected to this pair of lines is turned on. The time-averaged heating power of each heater zone can be individually tuned by time-domain multiplexing. In order to prevent crosstalk between different heater zones, a rectifier **250** (e.g. a diode) may be serially connected between each heater zone and the power supply lines connected thereto (as shown in Fig. 2), or between each heater zone and the power return lines connected thereto (not shown). The rectifier can be physically located in the heating plate or any suitable location. Alternatively, any current blocking arrangement such as solid state switches can be used to prevent crosstalk.

[0030] Figs. 3A, 3B and 3C show a substrate support assembly comprising an ESC, a cooling plate, and one embodiment of the heating plate wherein the heater zones **101** and power supply lines **201** are arranged in a first plane **302**, and the power return lines **202** are arranged in a second plane **303** separated from the first plane **302** by an electrically insulating layer **304**. The power return lines **202** are connected to the heater zones **101** by conductive vias **301** in the electrically insulating layer **304**, extending between the first plane **302** and the second plane **303**.

[0031] In use, the power supply lines **201** and power return lines **202** are connected to circuitry external to the heating plate through holes or conduits in the cooling plate. It should be appreciated that the presence of holes or conduits in the cooling plate can affect the temperature uniformity of substrate support assembly adversely, therefore reducing the number of holes or conduits in the cooling plate can enhance temperature uniformity. In addition, a small number of holes makes placing them around the edge of the substrate support assembly possible. For example, a single power supply conduit in the cooling plate can be used to feed

electrical leads to the power supply lines **201**. In one embodiment (Fig. 4A and 4B), the heater zones **101** and power supply lines **201** are arranged in a first plane **402**. The power supply lines **201** are connected to leads **404** in a second plane **403** through conductive vias **301** extending between the first plane **402** and the second plane **403**. The second plane **403** is separated from the first plane **402** by an electrically insulating layer (not shown). The power return lines **202** are arranged in the second plane **403** and are connected to the heater zones **101** through conductive vias **301** extending between the first plane **402** and the second plane **403**. In the second plane **403**, the leads **404** are brought through a hole or conduit **401** in the cooling plate while maintaining electrical insulation between the leads. Similarly, the power return lines **202** are connected to leads **405** brought through a hole or conduit **406** in the cooling plate while maintaining electrical insulation between the leads **405**.

[0032] Figs. 5A, 5B, 5C and 5D show a substrate support assembly comprising yet another embodiment of the heating plate, the heater zones **101** are arranged in a first plane **501**; the power supply lines **201** are arranged in a second plane **502**; and the power return lines **202** are arranged in a third plane **503**. The first plane **501**, second plane **502** and third plane **503** are separated from each other by electrically insulating layers **504** and **304**. The power supply lines **201** and power return lines **202** are connected to the heater zones **101** through conductive vias **301** in the electrically insulating layers **304** and **504**, extending between the planes **501**, **502** and **503**. Leads (not shown) connected to the power supply lines **201** are routed through holes or conduits **505** in the layer **504**. It should be appreciated that the planes **501**, **502** and **503** may be arranged in any order in the vertical direction, provided that the vias and conduits are suitably arranged. Preferably, the heaters are arranged closest to the substrate support assembly upper surface. Fig. 5E shows an embodiment wherein each heater zone **101** is connected to the power return line **202** through a rectifier **506** (e.g. a diode). The rectifier **506** only allows electric current flowing from the power supply line **201** through the heater zone **101** to the power return line **202**, and thus prevents crosstalk between heater zones.

[0033] The substrate support assembly can comprise an additional electrically insulating layer **604** in which one or more additional heaters (hereafter referred to as

primary heaters **601**) are incorporated (Fig. 6). Preferably, the primary heaters **601** are individually controlled high-power heaters. The power of the primary heaters is between 100 and 10000W, preferably, between 1000 and 5000W. The primary heaters may be arranged as a rectangular grid, concentric annular zones, radial zone or combination of annular zones and radial zones. The primary heaters may be used for changing the mean temperature, tuning the radial temperature profile, or step-by-step temperature control on the substrate. The primary heaters may be located above or below the heater zones of the heating plate.

[0034] In one embodiment, at least one of the insulating layers in the heating plate is a sheet of polymer material.

[0035] In another embodiment, at least one of the insulating layers in the heating plate is a sheet of inorganic material such as ceramic or silicon oxide. Examples of suitable insulating and conductive material for use in manufacture of ceramic chucks are disclosed in commonly assigned U.S. Patent No. 6483690, the disclosure of which is hereby incorporated by reference.

[0036] A substrate support assembly can comprise an embodiment of the heating plate, wherein each heater zone of the heating plate is of similar size to or smaller than a single device die or group of device dies on the substrate so that the substrate temperature, and consequently the plasma etching process, can be controlled for each device die position to maximize the yield of devices from the substrate. The scalable architecture of the heating plate can readily accommodate the number of heater zones required for die-by-die substrate temperature control (typically more than 100 dies on a substrate of 300-mm diameter) with minimal number of power supply lines, power return lines, and feedthroughs in the cooling plate, thus reduces disturbance to the substrate temperature, the cost of manufacturing and complexity of the substrate support assembly. Although not shown, the substrate support assembly can comprise features such as lift pins for lifting the substrate, helium back cooling, temperature sensors for providing temperature feedback signals, voltage and current sensors for providing heating power feedback signals, power feed for heaters and/or clamp electrode, and/or RF filters.

[0037] In one embodiment of the method for manufacturing the heating plate, where the insulating layers are ceramic, the insulating layers may be formed by

depositing the ceramic on a suitable substrate using techniques such as plasma spraying, chemical vapor deposition or sputtering. This layer can be an initial starting layer or one of the insulating layers of the heating plate.

[0038] In one embodiment of the method for manufacturing the heating plate, where the insulating layers are ceramic, the insulating layers may be formed by pressing a mixture of ceramic powder, binder and liquid into sheets and drying the sheets (hereafter referred as green sheets). The green sheets can be about 0.3 mm in thickness. The vias may be formed in the green sheets by punching holes in the green sheets. The holes are filled with a slurry of conducting powder. The heater elements, power supply and power return lines may be formed by: screen printing a slurry of conducting powder (e.g. W, WC, doped SiC or $MoSi_2$), pressing a precut metal foil, spraying a slurry of conducting powder, or any other suitable technique. Recesses for accommodating any rectifiers such as diodes may be pressed during the forming process of the green sheets or cut in the green sheets after the forming process. Discrete component rectifiers may be mounted into these recesses. Multiple green sheets with a variety of components (power lines, vias, rectifiers and heater elements) are then aligned, pressed and sintered to form an entire heating plate.

[0039] In another embodiment of the method for manufacturing the heating plate, where the insulating layers are ceramic, the insulating layers may be formed by pressing a mixture of ceramic powder, binder and liquid into green sheets and drying the green sheets. The green sheets can be about 0.3 mm in thickness. Holes are punched in the green sheets for accommodating vias. Recesses for accommodating any rectifiers such as diodes may be pressed during the forming process of the green sheets or cut in the green sheets after the forming process. Then, individual green sheets are sintered. The holes in the sintered sheets for accommodating vias are filled with a slurry of conducting power. The heater elements, power supply and power return lines may be screen printed with a slurry of conducting powder (e.g. W, WC, doped SiC or $MoSi_2$), or be formed using any other suitable technique, on the sintered sheets. Discrete component rectifiers may be mounted into the recesses in the sintered sheets. Multiple sintered sheets with a variety of components (lines,

vias, rectifiers and heater elements) are then aligned and bonded with an adhesive to form an entire heating plate.

[0040] In one embodiment where the insulating layers are silicon oxide sheets, the insulating layers may be formed by depositing a thin film silicon oxide onto a suitable substrate using techniques such as evaporation, sputtering, PVD, CVD, PECVD.

[0041] In one preferred embodiment of the method for manufacturing the heating plate, a thin metal sheet (component layer) such as Al, Inconel® or Cu foil, is bonded (e.g. heat pressed, adhered with adhesive) to a first polymer film such as polyimide. A patterned resist film is applied to the surface of the component layer wherein the patterns define the shapes and positions of the electrical components such as heater elements, power supply lines or power return lines. The exposed metal is chemically etched and the resist pattern is retained in the remaining metal sheet. The resist is then removed by dissolution in a suitable solvent or dry stripping. A second polymer film with holes for accommodating vias (via layer) is aligned and bonded to the first polymer film. The sidewalls of the holes may be coated by plating metal therein. Any suitable number of component layers and via layers may be incorporated serially. Finally, exposed metal components are covered by a continuous polymer film for electrical insulation.

[0042] In another embodiment, the heater elements, power supply and power return lines are made of metal films deposited (e.g. plasma sprayed, electroplated, chemical vapor deposition, or sputtered) on an insulating layer or substrate (e.g. a green sheet).

[0043] In another embodiment, the heater elements, power supply and power return lines are made of a thin layer of amorphous conductive inorganic film such as indium tin oxide deposited (e.g. electroplated, chemical vapor deposition, or sputtered) on an insulating layer or substrate (e.g. a green sheet).

[0044] In yet another embodiment, the heater elements, power supply and power return lines are made of a thin layer of conductive ceramic film deposited (e.g. chemical vapor deposition, or sputtered) on an insulating layer or substrate (e.g. a green sheet).

[0045] In one embodiment, the power supply and power return lines in the heating plate may be connected to the external circuitry by terminal connectors such as spring tipped passthroughs embedded in but electrically insulated from the cooling plate.

[0046] In another embodiment, the power supply and power return lines in the heating plate may be connected to the external circuitry by attaching (soldered, bonded with conductive adhesive or spot welded) lead wires to the power supply and power return lines and threading these lead wires through holes or conduits in the cooling plate.

[0047] In a plasma processing system, the RF power applied in the plasma processing chamber is usually above 100W, sometimes above 1000W. The amplitude of RF voltages can exceed a kilovolt. Such strong RF power can easily affect the operation of the control and power circuit of the heater zones without proper filtration or isolation. An RF filter can be used to shunt the RF power away from the control and power circuit. An RF filter may be a simple broad-band filter or a tuned-filter for the specific RF frequencies used in the plasma processing system. An RF isolator, in contrast, eliminates direct electrical connection between any RF-coupled components and the control and power circuit. An RF isolator may be an optical coupler or a transformer.

[0048] As an overview of how a plasma processing chamber operates, Fig. 7A shows a schematic of a plasma processing chamber comprising a chamber **713** in which an upper showerhead electrode **703** and a substrate support assembly **704** are disposed. A substrate **712** is loaded through a loading port **711** onto the substrate support assembly **704**. A gas line **709** supplies process gas to the upper showerhead electrode **703** which delivers the process gas into the chamber. A gas source **708** (e.g. a mass flow controller power supplying a suitable gas mixture) is connected to the gas line **709**. A RF power source **702** is connected to the upper showerhead electrode **703**. In operation, the chamber is evacuated by a vacuum pump **710** and the RF power is capacitively coupled between the upper showerhead electrode **703** and a lower electrode in the substrate support assembly **704** to energize the process gas into a plasma in the space between the substrate **712** and the upper showerhead electrode **703**. The plasma can be used to etch device die features into layers on the

substrate **712**. The substrate support assembly **704** may have heaters incorporated therein. It should be appreciated that while the detailed design of the plasma processing chamber may vary, RF power is coupled through the substrate support assembly **704**.

[0049] Fig. 7B shows a schematic of an embodiment of RF filtration or isolation, wherein no filters or isolators are connected on the heater zone power supply and power return lines and the control and power circuit **705** is connected to a filter or isolator **706B**, which is connected to the electric ground **701**. The primary heaters (not shown), if present in the substrate support assembly, preferably have separate filters or isolators due to their high power. In this approach, the control and power circuit **705** floats at the RF potential or "high side". This approach allows multiple heater zones to share only one filter or isolator.

[0050] All the high side circuitry can be housed inside a local floating Faraday cage immediately under the substrate support assembly base structure.

[0051] Alternatively, an isolation transformer is used as the single filter or isolator **706B** to isolate the power and control circuitry **705** from the RF. The control and power circuitry **705** of the heater zones should be capable of operating at relatively high frequency (25 to 250KHz) because the transformer strongly attenuates DC and low frequency transmission. The control and power circuitry is referenced to a single floating potential (floating ground). This requires that the control and power circuitry connected to this isolation transformer must be subject to very similar RF exposure. If the RF potentials differ substantially between two groups of control and power circuits, significant RF current flows between these groups. In this scenario, each group must have its own filter or isolator, or there must be a filter or isolator between these groups.

[0052] The filter or isolator **706B** may be physically located in the plasma processing chamber or any other suitable location.

[0053] One embodiment of the heater control electronics is depicted in Fig. 8. A low side controller **809** may be a microcontroller unit (MCU) or a higher level device such as a computer (PC). Through an optical coupler **807**, the low side controller communicates digitally to the high side MCU **805** which interacts with the heater zones **801**, sensors **803**, and any auxiliary circuits **802**. If the high side MCU

805 has sufficient capability and local memory, any set-point and program may be preloaded into the high side MCU **805** before each run, thus eliminating the need of a real-time link to the low side controller **809**. **804** represents one-way communication links between modules. **806** represents two-way communication links between modules.

[0054] In one embodiment of time-domain multiplexing schemes, the high side MCU supplies power to each heater zone power supply line sequentially. Only one power supply line is connected to a power supply at the same time. During the time when one power supply line is powered, the high side MCU may keep any or all power return lines connected to the floating reference for a portion of this duration. A heater zone is turned on when at least one of the power supply lines connected to this heater zone is connected to the power supply, and at least one of the power return lines connected to this heater zone is connected to the floating reference. The average power of a heater zone is directly proportional to the average duration it is turned on. Alternatively, during the time when one power supply line is powered, the high side MCU may keep any or all power return lines connected to the floating reference for this entire duration and regulate the power transmitted to each heater zone that is turned on.

[0055] For example, with a 10-by-10 grid of heater zones, heater zones in row number N are connected to a power supply line number N; heater zones in column number M are connected to a power return line number M. The high side MCU may control heating such that each of the power supply lines is connected to the power supply for 100 ms, sequentially. For example, during the 100 ms of time when power supply line number 3 is connected to the power supply, the MCU is operable to connect power return lines number 7, 8, and 9 to the floating reference for 10, 50 and 100 ms, respectively, as directed by the particular heating requirement during this 100 ms. Thus, the heater zone in row number 3 and column number 7 has a duty cycle of 1%; the heater zone in row number 3 and column number 8 has a duty cycle of 5%; the heater zone in row number 3 and column number 9 has a duty cycle of 10%. In this particular example, the maximum peak power for each heater zone would be set to ten times the average maximum power desired.

[0056] In order to prevent detectable temperature modulation, the switching frequencies and the entire multiplexing scheme are preferably sufficiently rapid that each heater zone gets addressed frequently (at least 1Hz). Additional loop control may be implemented using feedback data from one of more temperature sensors. Voltage and current sensors can also be implemented if desired. These sensors can be configured to measure parameters such as temperatures on different locations on the substrate and power of heater zones. These measured parameters are sent to the control and power circuit to be compared with set targets of these parameters so that the control and power circuit can adjust the power delivered to the heater zones accordingly in order to minimize the difference between the measured parameters and their set targets.

[0057] While a heating plate, methods of manufacturing the heating plate, a substrate support assembly comprising the heating plate, and a method of using a plasma processing chamber containing the substrate support assembly have been described in detail with reference to specific embodiments thereof, it will be apparent to those skilled in the art that various changes and modifications can be made, and equivalents employed, without departing from the scope of the appended claims. For instance, the substrate support assembly can include temperature sensors for monitoring substrate temperature, a power feed arrangement to power the ESC with desired clamping voltage, a lifting pin arrangement for raising and lowering a substrate, a heat transfer gas feed arrangement for supplying gas such as helium to the underside of the substrate, a temperature controlled liquid feed arrangement to supply heat transfer liquid to the cooling plate, a power feed arrangement to individually power primary heaters above or below the planar heater zones, a power feed arrangement to supply RF power at one or more frequencies to a lower electrode incorporated in the substrate support assembly, and the like.

We Claim:

1. A substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, comprising:

an electrostatic chuck (ESC) including an electrostatic clamping layer having at least one clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly;

a heating plate arranged below the electrostatic clamping layer;

a cooling plate attached to a lower side of the heating plate by a thermal barrier layer;

the heating plate comprising:

a first electrically insulating layer;

planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones; and

wherein (a) the power supply lines are connected to leads electrically insulated from each other and extended through at least one power supply conduit in the cooling plate and the power return lines are connected to leads electrically insulated from each other and extended through at least one power return conduit in the cooling plate; or (b) the power supply lines and power return lines are connected to terminal connectors embedded in the cooling plate.

2. The substrate support assembly of claim 1, wherein

(a) the planar heater zones and the power supply lines are in a first plane; the power return lines are in a second plane parallel to the first plane; the first and second planes are separated from one another by the first electrically insulating layer; the power return lines are electrically connected to the planar heater zones by vias extending vertically in the first electrically insulating layer;

(b) the planar heater zones and the power return lines are in a first plane; the power supply lines are in a second plane parallel to the first plane; the first and second planes are separated from one another by the first electrically insulating layer; the power supply lines are electrically connected to the planar heater zones by vias extending vertically in the first electrically insulating layer; or

(c) the planar heater zones are in a first plane; the power supply lines are in a second plane parallel to the first plane; the power return lines are in a third plane parallel to the first plane; the first and second planes are separated by the first electrically insulating layer; the second and third planes are separated by a second electrically insulating layer; the power supply lines and power return lines are electrically connected to the planar heater zones by vias extending through the electrically insulating layers.

3. The substrate support assembly of claim 1, wherein the planar heater zones are sized such that:

(a) each planar heater zone is not larger than four device dies being manufactured on the semiconductor substrate, or

(b) each planar heater zone is not larger than two device dies being manufactured on the semiconductor substrate, or

(c) each planar heater zone is not larger than one device die being manufactured on the semiconductor substrate, or

(d) the area of each planar heater zone is between 2 and 3 square centimeters, or

(e) the heating plate includes 100 to 400 planar heater zones, or

(f) each planar heater zone is 1 to 15 cm^2, or

(g) each planar heater zone is 16 to 100 cm^2, or

(h) each planar heater zone is scaled with sizes of device dies on the semiconductor substrate and the overall size of the semiconductor substrate.

4. The substrate support assembly of claim 1, wherein the first electrically insulating layer comprises a polymer material, a ceramic material, or a combination thereof.

5. The substrate support assembly of claim 1, wherein the total number of the power supply lines and the power return lines is equal to or less than the total number of the planar heater zones.

6. The substrate support assembly of claim 1, wherein a total area of the planar heater zones is from 50% to 90% of an upper surface of the heating plate.

7. The substrate support assembly of claim 1, wherein the planar heater zones are arranged in a rectangular grid, hexagonal grid or concentric rings; and the planar heater zones are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

8. The substrate support assembly of claim 1, wherein a rectifier is serially connected between each heater zone and the power supply line connected thereto, or a rectifier is serially connected between each heater zone and the power return line connected thereto.

9. The substrate support assembly of claim 8, wherein the rectifier is a semiconductor diode.

10. The substrate support assembly of claim 1, further comprising a control and power circuit operable to selectively supply power at any given time to (a) only the first heater zone, (b) only the second heater zone, (c) only the third heater zone, (d) only the fourth heater zone, (e) only the first and second planar heater zones, (f) only the first and third planar heater zones, (g) only the second and fourth planar heater zones, (h) only the third and fourth planar heater zones, and (i) all of the planar heater zones.

11. The substrate support assembly of claim 10, further comprising at least one filter or isolator serially connected between the control and power circuit and electric ground.

12. The substrate support assembly of claim 11, wherein the at least one filter or isolator is a transformer.

13. The substrate support assembly of claim 1, further comprising at least one primary heater layer arranged above or below the first electrically insulating layer of the heating plate, wherein the primary heater layer is electrically insulated from the planar heater zones, the power supply lines, and the power return lines of the heating plate; the primary heater layer includes at least one heater which provides mean temperature control of the semiconductor substrate; the planar heater zones provide radial and azimuthal temperature profile control of the semiconductor substrate, during processing thereof.

14. The substrate support assembly of claim 1, wherein the terminal connectors are spring-tipped passthroughs.

15. The substrate support assembly of claim 13, wherein the primary heater layer includes two or more heaters.

16. A heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate, and

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber.

17. A substrate support comprising:

a heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more

power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate, and

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber;

a switching device which independently supplies power to each one of the heater zones via one of the power supply lines and one of the power return lines to provide time-averaged power to each of the heater zones by time divisional multiplexing of the switches; and

a temperature controlled and radio frequency (RF) powered base plate beneath the heating plate and high side circuitry housed in local faraday cage under the base plate.

18. A heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate;

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber;

the heating plate includes a first electrically insulating layer with planar heater zones distributed laterally across the first electrically insulating layer and comprising at least first, second, third and fourth planar heater zones, each planar heater zone having one or more heater elements;

the power supply lines comprise at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; and

the power return lines comprise at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones.

19. The heating plate of claim 16, wherein the heating plate is incorporated in a substrate support which includes temperature sensors configured to measure temperature at locations on the semiconductor substrate; and

a control and power circuit connected to the array of heater zones and configured to receive the measured parameters from the temperature sensors and adjust power delivered to the heater zones to minimize differences between the measured parameters and set targets.

20. The substrate support of claim 17, further comprising:

an isolator connected to electric ground,

wherein the switching device is connected to the isolator.

21. The substrate support of claim 20, wherein the switching device is located in a plasma etching chamber.

22. The substrate support of claim 20, wherein the isolator is an isolation transformer that isolates the switching device from RF.

23. A heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate;

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber;

the heater zones are supported on a first electrically insulating layer;

the second layer is arranged above or below the first electrically insulating layer; and

the one or more primary heaters are electrically insulated from the array of heater zones, the power supply lines, and the power return lines.

24. The substrate support of claim 17, wherein the switching device is a high side controller that floats at an RF potential, the substrate support further comprising:

an optical coupler connected to the high side controller for digital communication with a low-side controller.

25. The substrate support of claim 17, wherein the switching device connects at least one power return line to a floating reference.

26. The substrate support of claim 17, wherein the switching device is configured to turn on one of the heater zones when at least one power supply line connected to the heater zone is connected to a power supply, and at least one power return line connected to the heater zone is connected to a floating reference.

27. The substrate support of claim 17, wherein the switching device connects all power return lines to a floating reference.

28. The substrate support of claim 17, wherein the switching device is configured to address each heater zone of the array of heater zones at a frequency of at least 1 Hz.

29. A substrate support comprising the heating plate of claim 16, wherein the substrate support includes sensors configured to measure parameters on different locations on the substrate support and power of the heater zones.

30. The substrate support of claim 29, wherein the sensors include at least one of voltage and current sensors.

31. The substrate support of claim 29, wherein the measured parameters include at least temperature measurements.

32. The substrate support of claim 17, wherein the switching device is configured to maintain a connection between all power return lines and a floating reference during a time when one power supply line is powered and regulate power transmitted to heat a heater zone that is turned on.

33. A substrate support, comprising:

a heating plate configured to provide radial and azimuthal temperature control of a semiconductor substrate supported on a semiconductor substrate support in a processing chamber, comprising:

a first layer having an array of heater zones operable to tune a spatial temperature profile on the semiconductor substrate, the heater zones powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to at least two of the heater zones and each power return line is connected to at least two of the heater zones, each heater zone not larger than four device dies being manufactured on the semiconductor substrate, and

a second layer having one or more primary heaters operable to provide mean temperature control of the semiconductor substrate during processing in the processing chamber; and

an electrostatic clamping (ESC) layer above the heating plate.

34. The substrate support of claim 33, further comprising a radio frequency (RF) powered base plate beneath the heating plate.

35. The heating plate of claim 16, wherein the heater zones comprise at least 100 independently controllable heater zones embedded in ceramic material.

36. A method for manufacturing a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate

comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, the method comprising:

(a) forming holes in ceramic sheets;

(b) printing a slurry of conductor powder, or pressing a precut metal foil, or spraying a slurry of conductor powder, on the ceramic sheets to form the planar heater zones, the power supply lines, and power return lines;

(c) filling the holes in the ceramic sheets with a slurry of conductor powder to form power supply and power return vias; and

(d) aligning, pressing and bonding the ceramic sheets to form the heating plate.

37. The method of claim 36, wherein the planar heater zones and power supply lines are formed on the upper side of a first ceramic sheet, the power return lines are formed on the lower side of the first ceramic sheet, a second ceramic sheet is placed over the upper surface of the first ceramic sheet and a third ceramic sheet is placed below the first ceramic sheet, and the first, second and third ceramic sheets are pressed together and sintered to form a joint-free heating plate.

38. A method for manufacturing a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically

connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, the method comprising:

manufacturing a component layer of the heating plate by:

(a) bonding a metal sheet onto a polymer film;

(b) etching the metal sheet to remove metal exposed through openings of a patterned film, the etching forming an electrically conductive metal pattern of at least one of the planar heater zones, power supply lines and power return lines; and

(c) removing the film;

manufacturing a via layer by:

(a) punching or cutting holes in a polymer film; and

(b) forming conductive vias in the holes;

building a laminate by bonding at least one manufactured component layer and at least one manufactured via layer; and

insulating the laminate by bonding a continuous polymer film onto at least one of upper and lower surfaces of the laminate.

39. A method for manufacturing a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, the method comprising:

depositing metal, amorphous conductive inorganic material, or conductive ceramic on the first electrically insulating layer to form at least one of the planar heater zones, power supply lines and power return lines.

40. A method for processing semiconductor substrates in a semiconductor processing apparatus containing a substrate support assembly comprising an electrostatic chuck (ESC) including an electrostatic clamping layer having at least one clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly; a heating plate arranged below the electrostatic clamping layer, the heating layer comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones; and a cooling plate attached to a lower side of the heating plate by a thermal barrier layer, the method comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly;

(b) determining a temperature profile for processing conditions affecting critical dimension (CD) uniformity

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support assembly;

(d) processing the semiconductor substrate while controlling the temperature profile by independently controlled heating of the planar heater zones;

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.

41. The method of claim 36, wherein the planar heater zones are formed on a first ceramic sheet, the power supply lines are formed on a second ceramic sheet placed below the first

ceramic sheet, the power return lines are formed on a third ceramic sheet placed below the second ceramic sheet, a fourth ceramic sheet is placed over the first ceramic sheet, and the first, second, third and fourth ceramic sheets are pressed together and sintered to form a joint-free heating plate.

42. The method of claim 41, wherein the first, second, third, and fourth ceramic sheets are aligned prior to being pressed together and sintered.

43. The method of claim 37, wherein the first, second, and third ceramic sheets are aligned prior to being pressed together and sintered.

44. The method of claim 36, comprising pressing or cutting recesses into the ceramic sheets formed into the heating plate and mounting rectifiers in the recesses.

45. The method of claim 36, comprising connecting a rectifier between each heater zone and the power supply line or power return line connected thereto.

46. A method for manufacturing a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising a first electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements, the planar heater zones laterally distributed across the first electrically insulating layer and operable to tune a spatial temperature profile on the substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, the method comprising:

forming a manufactured component layer of the heating plate by:

(a) bonding a sheet onto a polymer film;

(b) applying a second film onto the sheet wherein openings in the second film correspond to locations where metal is to be removed;

(c) etching the sheet to remove portions of the sheet exposed through openings of the second film, the etching forming an electrically conductive pattern of at least one of the planar heater zones, power supply lines and power return lines; and

(d) removing the second film;

forming a manufactured via layer by:

(a) punching or cutting holes in a polymer film; and

(b) forming conductive vias in the holes;

building a laminate by bonding at least one manufactured component layer and at least one manufactured via layer; and

insulating the laminate by bonding a continuous polymer film onto at least one of upper and lower surfaces of the laminate.

47. The method of claim 46, wherein the sheet is a conductive inorganic film.

48. The method of claim 46, wherein the sheet is a conductive ceramic sheet.

49. The method of claim 36, wherein the ceramic sheets are green sheets and the bonding comprises sintering the green sheets.

50. The method of claim 39, wherein the depositing comprises sputtering, PVD, CVD, PECVD, plasma spraying or electroplating.

51. The method of claim 36, wherein the heating plate includes 100 to 400 planar heater zones, each planar heater zone covers 1 to 15 cm^2 or each planar heater zone covers 16 to 100 cm^2.

52. The method of claim 36, wherein a total area of the planar heater zones is from 50 to 90% of the upper surface of the heating plate.

53. The method of claim 36, further comprising arranging a primary heater layer above or below the planar heater zones, the primary heater layer including one or more primary heaters powered by 100 to 10,000 W and each of the planar heater zones powered by less than 20 W.

54. The method of claim 36, further comprising attaching the heating plate to a cooling plate and connecting the power supply and power return lines to terminal connectors.

55. The method of claim 36, wherein the layers are bonded with adhesive.

56. The method of claim 36, further comprising forming a substrate support assembly by attaching the heating plate and an electrostatic chuck to a lower electrode.

57. A method of powering heaters in a substrate support assembly on which a semiconductor substrate is supported, the support assembly having an array of heaters powered by two or more power supply lines and two or more power return lines wherein each power supply line is connected to a power supply and at least two of the heaters and each power return line is connected to at least two of the heaters, and a switching device which independently connects each one of the heaters to one of the power supply lines and one of the power return lines so as to provide time-averaged power to each of the heaters by time divisional multiplexing of switches of the switching device, the method comprising:

supplying power to each of the heaters sequentially using a time-domain multiplexing scheme.

58. The method of claim 57, wherein only one power supply line is connected to a power supply at the same time.

59. The method of claim 57, wherein an average power of each of the heaters is directly proportional to an average duration of time that heater is turned on.

60. The method of claim 57, wherein the array of heaters are arranged in a grid, the method further comprising:

connecting heaters in row number N with a power supply line number N; and

connecting heaters in column M connected to a power return line number M.

61. The method of claim 57, further comprising:

sequentially connecting each of the power supply lines to a power supply.

62. The method of claim 57, further comprising:

addressing each heater at a frequency of at least 1 Hz.

63. The method of claim 57, wherein:

measuring, via sensors, parameters of the substrate and the heaters;

sending the measured parameters to a control and power circuit; and

adjusting power delivered to the heaters to minimize differences between the measured parameters and set targets.

64. The method of claim 57, wherein the substrate support includes a control and power circuit, the method further comprising:

sequentially supply power, via the control and power circuit, to at least 16 heaters.

65. The method of claim 57, wherein at least one primary heater layer is arranged above or below a first electrically insulating layer of a heating plate supporting the heaters, wherein the primary heater layer is electrically insulated from the heaters, the power supply lines, and the power return lines; the primary heater layer includes at least one heater which provides mean temperature control of the semiconductor substrate; the heaters provide radial and azimuthal temperature profile control of the semiconductor substrate, the method comprising:

powering the primary planar heater layer to a predetermined temperature; and

plasma processing the semiconductor substrate at the predetermined temperature.

66. The method of claim 57, further comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly;

(b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity;

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support assembly;

(d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled heating of the heaters; and

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.

67. The method of claim 66, wherein the processing comprises plasma etching the semiconductor substrate.

68. The method of claim 57, further comprising:

supplying one power supply line with power; and

during the supply of power to the one power supply line:

selecting return lines to be activated; and

connecting a plurality of the selected return lines to a floating reference for identical or different time durations to regulate power supplied to heaters connected to the power supply line and the selected return lines.

69. The method of claim 57, wherein the heaters are sized such that:

(a) each heater is not larger than four device dies being manufactured on the semiconductor substrate, or

(b) each heater is not larger than two device dies being manufactured on the semiconductor substrate, or

(c) each heater is not larger than one device die being manufactured on the semiconductor substrate, or

(d) the area of each heater is between 2 and 3 square centimeters, or

(e) the heater array includes 100 to 400 planar heaters, or

(f) each heater heats a planar heater zone of 1 to 15 cm^2, or

(g) each heater heats a planar heater zone of 16 to 100 cm^2, or

(h) each heater is scaled with sizes of device dies on the semiconductor substrate and the overall size of the semiconductor substrate.

70. The method of claim 57, wherein the total number of the power supply lines and the power return lines is equal to or less than the total number of the heaters.

71. The method of claim 57, wherein the heaters are arranged in a rectangular grid, hexagonal grid or concentric rings; and the heaters are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

72. The method of claim 57, wherein a rectifier is serially connected between each heater and the power supply line connected thereto, or a rectifier is serially connected between each heater and the power return line connected thereto.

73. The method of claim 57, wherein the heaters are resistive heaters and the maximum power supplied to the resistive heaters is 20 W.

74. The method of claim 57, further comprising: individually tuning a time averaged heating power of each heater by the time-domain multiplexing.

75. The method of claim 57, wherein the substrate support assembly includes primary heaters powered with 100 to 10,000 W, the primary heaters located below the array of heaters.