

SOLAR CELL FABRICATION USING IMPLANTATION

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application claims priority to co-pending U.S. Provisional Application Serial Number 61/131,687, filed June 11, 2008, entitled "SOLAR CELL FABRICATION USING IMPLANTATION," co-pending U.S. Provisional Application Serial Number 61/131,688, filed June 11, 2008, entitled "APPLICATIONS SPECIFIC IMPLANT SYSTEM FOR USE IN SOLAR CELL FABRICATIONS," co-pending U.S. Provisional Application Serial
10 Number 61/131,698, filed June 11, 2008, entitled "FORMATION OF SOLAR CELL-SELECTIVE EMITTER USING IMPLANTATION AND ANNEAL METHODS," co-pending U.S. Provisional Application Serial Number 61/133,028, filed June 24, 2008, entitled "SOLAR CELL FABRICATION WITH FACETING AND IMPLANTATION," and co-pending U.S. Provisional Application Serial Number 61/210,545, filed March 20, 2009,
15 entitled "ADVANCED HIGH EFFICIENCY CRYSTALLINE SOLAR CELL FABRICATION METHOD," which are all hereby incorporated by reference as if set forth herein.

FIELD OF THE INVENTION

20 The present invention relates to the field of solar cells. More particularly, the present invention relates to a solar cell device and method of making.

BACKGROUND

25 The use of diffusion in forming dopants on the surface of a semiconductor substrate is plagued by several problems. One problem is excess accumulation of unactivated dopants near the surface as the dopants are driven into the bulk of the semiconductor material. This excess accumulation can vary the resistivity in different regions of the semiconductor substrate and thus lead to varying light absorption capability and varying electron-hole formation and recombination performance of a solar cell. In particular, one problem
30 encountered is the lack of utilization of the blue light as the result of formation of a "dead layer."

 Another drawback of conventional diffusion forming systems is the difficulty in laterally positioning of the dopants across the semiconductor substrate as the line widths and wafer thicknesses become smaller. The solar cell industry is expected to require dopant
35 lateral placements, as emitter dimensions shrink from 200 microns down to less than 50

microns. Such miniaturization is difficult or even impossible for the present methodology of diffusion and screen printing in forming solar cells. Selectively altering the resistivity of regions underneath the metal grid lines with respect to the regions in between the grid lines provides charge collection and generation advantages and thus lead to gain in efficiencies.

Diffusion processes typically use a dopant material that is applied as a paste or sprayed onto the surface of the semiconductor substrate. The semiconductor substrate is then heated to drive the dopant to a particular depth to form a junction. The semiconductor substrate is typically heated in a diffusion furnace or a similar heating means. An n-type or p-type of a dopant can be used to form the junction depending upon the background doping type. A subsequent screen printing step is used to form contact lines onto the surface of the wafer in completing the solar cell.

The interface of the metal contact with the semiconductor affects the performance of the solar cell. Conventionally, the junction between the metal contact and the silicon is heated to form a silicide. This heating process improves the interface, but also includes drawbacks.

Accordingly, it is desirable to provide an improved more economical method of forming a solar cell to overcome the drawbacks of conventional solar cell manufacturing methods, allow production of solar cells with smaller dimensions and having tighter control of the dose and dopant position.

SUMMARY OF THE INVENTION

In accordance with a first aspect of the present invention, a solar cell device is provided. The device includes a silicon substrate including a preexisting dopant. A homogeneous lightly doped region is formed on a surface of the silicon substrate over the preexisting dopant. A junction is formed between the preexisting dopant and the lightly doped region. The junction is formed a predetermined distance from the surface of the silicon substrate. A heavily doped region is selectively implanted on the surface of the silicon substrate within the lightly doped region. A seed layer is formed over the heavily doped region. A metal contact is formed over the seed layer. The device can include an anti-reflective coating.

In an exemplary embodiment, the device includes the homogeneous lightly doped region having a resistivity in a range of 80 to 160 Ohms/square and the heavily doped region having a resistivity in a range of 10 to 40 Ohms/square. In one embodiment, the homogeneous lightly doped region includes a resistivity of approximately 100 Ohms/square and the heavily doped region includes a resistivity of approximately 25 Ohms/square. The

heavily doped regions can each be a width on the silicon substrate a distance in the range 50 to 200 microns. Also, the heavily doped regions can be laterally spaced on the silicon substrate a distance in the range 1 to 3 mm from each other.

The seed layer can be a silicide. The seed layer can also be a layer of a material including any of the materials Ni, Ta, Ti, W or Cu. The silicon substrate can include fiducial markers configured for aligning the placement of the heavily doped regions during an ion implantation process.

In accordance with a second aspect of the present invention, a method of forming a solar cell device is provided. The method includes providing a silicon substrate including a preexisting dopant. An ion implantation process is used to form a homogeneous lightly doped region on a surface of the silicon substrate over the preexisting dopant. A junction is formed between the preexisting dopant and the lightly doped region. The junction is formed a predetermined distance from the surface of the silicon substrate. A selective ion implantation process is used to form a heavily doped region implanted on the surface of the silicon substrate within the lightly doped region. The heavily doped region is implanted at predetermined locations on the silicon substrate surface. The selective ion implantation process is used to form a seed layer over the heavily doped region. A metal contact is formed over the seed layer. The method can include forming an anti-reflective coating.

The heavily doped region is implanted at predetermined locations on the silicon substrate surface using a physical mask. The physical mask includes openings aligned with the predetermined locations. The physical mask is formed on the surface of the silicon substrate. The physical mask is positioned at a predetermined distance above the surface of the silicon substrate during the selective ion implantation process to form the heavily doped region. In an alternative embodiment, the selective ion implantation process uses a shaped ion beam that is aligned with the predetermined locations to form the heavily doped region. In a further embodiment, such selective implantation can be done through a mask on the surface of the substrate. A combination of all the above embodiments of forming the heavily doped regions can be used.

In an exemplary embodiment, the homogeneous lightly doped region includes a resistivity in a range of 80 to 160 Ohms/square and the homogeneous lightly doped region includes a resistivity of approximately 100 Ohms/square. The heavily doped region can include a resistivity in a range of 10 to 40 Ohms/square. In one embodiment, the heavily

doped region includes a resistivity of approximately 25 Ohms/square. The heavily doped regions each include a width on the silicon substrate a distance in the range 50 to 200 microns and the heavily doped regions are laterally spaced on the silicon substrate a distance in the range 1 to 3 mm from each other.

5 The seed layer is preferably a silicide. The seed layer can be a layer of a material including any of the materials Ni, Ta, Ti, W or Cu. The silicon substrate can include fiducial markers configured for aligning the placement of the heavily doped regions during the selective ion implantation process. The method includes using an annealing process on the silicon substrate having the homogeneous lightly doped region. Alternatively, the annealing
10 process is used on the silicon substrate after forming the metal contact. Using annealing after forming the metal contact allows for lower temperature annealing than conventional processes. Thus allowing for the use of substrates or thin substrates on carriers that otherwise may degrade at higher temperatures.

Other features of the present invention will become apparent from consideration of
15 the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features of the invention are set forth in the appended claims. However, for purposes of explanation, several embodiments of the invention are set forth in the
20 following figures.

Figure 1 illustrates a method of making a selective emitter structure of a solar cell in accordance with an embodiment of the invention.

Figure 2 illustrates a method of making a selective emitter structure of a solar cell in accordance with an alternative embodiment of the invention.

25 Figure 3 illustrates a method of making a selective emitter structure of a solar cell in accordance with still another embodiment of the invention.

Figure 4 illustrates a method of forming a seed layer of a solar cell in accordance with an embodiment of the invention.

30 Figure 5 illustrates a method of forming a contact layer of a solar cell in accordance with an embodiment of the invention.

Figure 6 illustrates a side view of a solar cell device in accordance with an embodiment of the invention.

Figure 7 illustrates a side view of a solar cell device in accordance with an alternative embodiment of the invention.

Figure 7A illustrates a side view of a solar cell device in accordance with still another embodiment of the invention.

Figure 8 illustrates a process flow diagram of forming a solar cell device in accordance with an embodiment of the invention.

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DETAILED DESCRIPTION

In the following description, numerous details and alternatives are set forth for the purpose of explanation. However, one of ordinary skill in the art will realize that the invention can be practiced without the use of these specific details. In other instances, well-known structures and devices are shown in block diagram form in order not to obscure the description of the invention with unnecessary detail.

The present invention uses implantation to form homogeneous and selective emitter regions. The present invention addresses the methods for the formation of solar cells and in particular formation of a selective emitter through a series of implantation processes. Presently, such ability to manipulate and place the dopant laterally is difficult with conventional diffusion or screen printing processes. The present invention selectively controls the resistance of gridlines, contacts, and selectively controls contact resistance of a metal/semiconductor interface. Moreover, the advantageous formation of a selective emitter with ion implantation allows improved performance for solar cell devices. The present invention can be applied to grown single or mono-crystalline, poly or multi-crystalline silicon as well as very thin silicon placed on a carrier (such as glass) or very thin film deposited silicon or other materials used for solar cell formation. The present invention can be extended to atomic species placement for any other material used in fabrication of junctions.

Figure 1, illustrates a method of making a selective emitter structure 105 (step 101D) using an implantation process according to an embodiment of the present invention. At the step 101A, a silicon substrate 101 is provided that is pre-doped with a dopant 102. The silicon substrate 101 comprises a wafer of mono or poly silicon material. In an exemplary embodiment, the silicon substrate comprises a 156 x 156 mm wafer. Other suitable substrates known to a person of ordinary skill can also be used for the silicon substrate 101. In an exemplary embodiment, the silicon substrate 101 includes a pre-doped material 102. The pre-doped material 102 is pre-doped with a p-type dopant, typically or alternatively an n-type dopant. The pre-doped material 102 can have a resistivity in the range of 0.5-1.5 Ohms/cm and atomic concentration of less than 5E16/cm-cube. An implantation system (not shown) with a high productivity is used for the formation of a homogeneous lightly doped region or homogeneous layer 104. Such an implantation system is the subject of a

co-pending Patent Application Serial No. XXXXXX, entitled, "Application Specific Implant System for Use in Solar Cell Fabrications," filed June 11, 2009, which is hereby incorporated in the entirety. The homogeneous layer 104 is a high resistivity region. The homogeneous layer 104 allows the formation of electron-hole pairs as the result of an incidence of light. In operation, the homogeneous layer 104 preferably uses a relatively low level of a dopant (high resistivity) to facilitate the formation of charge carriers while avoiding recombination and thus avoiding the "dead layer" effect.

An ion beam 'A' is used for the implantation of the homogeneous layer 104. The ion beam A implants the homogeneous layer 104 in a blanket fashion in the pre-doped material 102. In implanting the homogeneous layer 104, either a spot beam or wide plasma beam is used to provide full coverage across the silicon substrate 101. The beam can be scanned across the wafer, the wafer can be moved under the beam or a combination thereof to achieve full coverage. A productivity of the implantation system comprises approximately 1000 or more wafers per hour.

A p-n junction 103 is formed where the pre-doped material 102 and the homogeneous layer 104 meet. The junction 103 can be formed a predetermined distance from a surface 107 of the silicon substrate 101. The distance of the junction 103 from the surface 107 is determined according to an amount of energy E1 used in the ion beam A. The amount of energy E1 can be in the range of 1 to 150 KeV depending on the desired specifications for the solar cell device. The homogeneous layer 104 can have a resistivity in the range of 80 to 160 Ohms/square. In an exemplary embodiment, the resistivity of the homogeneous layer 104 comprises approximately 100 Ohms/square. An anneal step can be performed here and is described in further detail below at the step 101C. Alternatively, the anneal step here can be eliminated until a final anneal step below (Figure 6).

At the step 101B, a contact mask 106 is formed on the surface 107 of the silicon substrate 101. The contact mask 106 allows selective placement of dopant in the silicon substrate 101 at predetermined locations. The contact mask 106 can be any suitable mask known to a person of ordinary skill. Examples of such masks can include photo-resist, a nitride layer, an oxide layer, a screen-printing or any other suitable film. The contact mask 106 can be formed using processes known to a person of ordinary skill. In one embodiment, a lithography or contact printing process can be used to form the contact mask 106. Openings 109 in the contact mask 106 can be a dimension as large as approximately 200

microns wide. Alternately, the openings 109 can be a dimension as small as 50 microns wide. A selective emitter 108 of the same size as the openings 109 can be formed by implanting dopant therethrough within the silicon substrate 101. A distance or pitch 111 (Step 101C) between each selective emitter 108 (Step 101C) can be in the range of approximately 1 mm to 3 mm.

The step 101C illustrates using an ion implantation beam 'B' for implanting a heavily doped region for the selective emitter 108. The ion beam B implants the selective emitter 108 in the homogeneous layer 104 that is not protected by the contact mask 106. The ion beam B can be applied in a blanket fashion over the whole silicon substrate 101 wherein the contact mask 106 will prevent ions from entering the substrate. Alternatively, the ion beam B can be applied in a targeted fashion using a shaped beam that is appropriately directed. Using the shaped beam can help reduce dopant usage and increase the implantation process productivity. The ion beam B includes a dopant that is chosen depending on the manufacturer specifications. In an exemplary embodiment, the dopant for the selective emitter 108 comprises an n-type dopant such as phosphorous or arsenic. Alternatively, the ion beam B can include a p-type dopant such as Boron in an embodiment that uses an n-type pre-doped material 102 for the silicon substrate 101. The selective emitter 108 is implanted to a depth and distance from the surface 107 into the pre-doped material 102. The distance of the selective emitter 108 from the surface 107 is determined according to an amount of energy E2 used in the ion beam B. The distance also depends on a dopant concentration level chosen for the ion beam B. The amount of energy E2 can depend on the desired specifications for the solar cell device. In an alternative embodiment, the step 101C includes multiple implantations using varying energy levels and varying dopant concentration levels of the ion beam B. In one embodiment, the energy E2 can be a continuum of variability to provide a tailored atomic profile. Such profile tailoring is described in further detail in a co-pending Patent Application Serial No. XXXXXX, entitled, "Formation of Solar Cell Selective Emitter Using Implant and Anneal Method," filed June 11, 2009, which is hereby incorporated in the entirety.

An annealing step heats the silicon substrate 101 to a temperature near but well below melting and restores any damage to the crystal structure of the silicon substrate 101 caused by the ion implantation. Also, such annealing will cause activation of dopant atoms. A temperature and time of such annealing and activation can be as low as 400-500 degrees Celsius, which is a sufficient temperature to eliminate any di-vacancies (missing atoms of a lattice structure of the silicon substrate 101) and to provide enough activation of the dopant atoms. The annealing step can comprise furnace annealing. Alternatively, a laser annealing

or flash lamp annealing can be used in place of the furnace annealing. The annealing step does not adversely affect subsequent process steps described below. In an alternative embodiment, this anneal step can be eliminated until the final anneal step below (Figure 6).

A surface texturing process can be included with the step 101C implantation of the selective emitter 108. Surface texturing provides a good light capture and adherence to the surface contour and thus will improve a contact formation that is described below. The selective emitter 108 can have a resistivity in the range of 10 to 40 Ohms/square. In an exemplary embodiment, the resistivity of the selective emitter 108 comprises approximately 25 Ohms/square.

The step 101D illustrates the completed selective emitter structure 105.

Figure 2, illustrates a method of making a selective emitter structure 205 (step 201C) using an implantation process according to an alternative embodiment of the present invention. Similar to that described above in Figure 1, at the step 201A, a silicon substrate 201 is provided that is pre-doped with a dopant 202. The silicon substrate 201 comprises a wafer of mono, poly or multi crystalline silicon material. In an exemplary embodiment, the silicon substrate comprises a 156 x 156 mm wafer. Other suitable substrates known to a person of ordinary skill can also be used for the silicon substrate 201. In an exemplary embodiment, the silicon substrate 201 includes a pre-doped material 202. The pre-doped material 202 is pre-doped with a p-type dopant. The pre-doped material 202 can have a resistivity in the range of 0.5-1.5 Ohms/cm and atomic concentration of less than 5×10^{16} /cm-cube. The implantation system as described above, includes a high productivity for the formation of a homogeneous lightly doped region or homogeneous layer 204. The homogeneous layer 204 is a high resistivity region. The purpose of the homogeneous layer 204 is the formation of electron-hole pairs as the result of an incidence of light. In operation, the homogeneous layer 204 requires a relatively low level of dopant (high resistivity) to facilitate the formation of charge carriers. An ion beam A is used for the implantation of the homogeneous layer 204. The ion beam A implants the homogeneous layer 204 in a blanket fashion in the pre-doped material 202. In implanting the homogeneous layer 204, either a spot beam or wide plasma beam is used to provide full coverage across the silicon substrate 201. A productivity of the implantation system comprises approximately 1000 or more wafers per hour.

A p-n junction 203 is formed where the pre-doped material 202 and the homogeneous layer 204 intersect. The junction 203 can be formed a predetermined distance from a surface 207 of the silicon substrate 201. The distance of the junction 203 from the surface 207 is determined according to an amount of energy E1 used in the ion beam A. The amount of

energy E1 can be in the range of 1 to 150 KeV depending on the desired specifications for the solar cell device. The homogeneous layer 204 can have a resistivity in the range of 80 to 160 Ohms/square. In an exemplary embodiment, the resistivity of the homogeneous layer 204 comprises approximately 100 Ohms/square. An anneal step can be performed here and is described in further detail below at the step 201B. Alternatively, the anneal step here can be eliminated until the final anneal step below (Figure 6).

At the step 201B a hard mask 206 is used to facilitate implantation of a selective emitter 208. The hard mask can be included in an implanter (not shown) of the implantation system (not shown). The hard mask 206 allows selective placement of dopant on the silicon substrate 201 at predetermined locations. The hard mask 206 can be any suitable material from which such mask are fabricated. The suitable material of the hard mask 206 does not affect the implantation process or the solar cell device through sputtering. The suitable material of the hard mask 206 is able to tolerate elevated temperatures experienced during the ion beam heating. In one embodiment, the hard mask 206 can comprise Silicon or SiC. However, a person of ordinary skill will appreciate many suitable other materials. A suitable thickness of the hard mask 206 allows control and management of the hard mask 206 temperature during heating and cooling of the hard mask 206. The placement and support of the hard mask 206 depends on the material and thickness chosen for the hard mask 206. The hard mask 206 can be placed on the wafer prior to the beginning of ion implantation. The hard mask 206 can be directly placed on the silicon substrate surface 207. Alternatively, a support or spacer (not shown) can be used to provide a gap between the hard mask and the silicon substrate surface 207. In another embodiment, the hard mask 206 can be an array placed off from the surface 207.

Openings 209 in the hard mask 206 can be a distance to produce the selective emitter 208 as large as approximately 200 microns wide. Alternately, the openings 209 can be adjusted or can be a distance to produce the selective emitter 208 as small as 50 microns wide. A distance or pitch 211 between each selective emitter 208 can be in the range of approximately 1 mm to 3 mm. A registration mark or fiducial markers can be scribed onto the silicon substrate 201 using the implantation system. The registration mark can be used for alignment of hard mask 206 with the silicon substrate 201. The registration marks can be used for alignment during subsequent steps of the implantation process of the selective emitter 208. In an alternative embodiment, a virtual center of the wafer is defined optically and the hard mask 206 and the wafer are accordingly aligned to provide a consistent and repeatable pattern on many wafers.

Still referring to the step 201B, an ion implantation beam 'C' for implanting a heavily doped region or the selective emitter 208 is shown. The ion beam C implants the selective emitter 208 in the homogeneous layer 204 that is not shadowed by the hard mask 206. The ion beam C can be applied in a blanket fashion over the whole silicon substrate 201 including the hard mask 206. Alternatively, the ion beam C can be applied in a targeted fashion using a shaped beam. Using the shaped beam can help reduce dopant usage and increase the implantation process productivity. In an exemplary embodiment, the ion beam C can comprise a broad shaped ion beam. In another embodiment, the ion beam C can comprise a moving spot ion beam. The broad shaped ion beam and the moving spot beam can be used to facilitate forming the selective emitter 208 approaching the width of 50 microns.

The ion beam C includes a dopant that is chosen depending on the manufacturer specifications. In an exemplary embodiment, the dopant for the selective emitter 208 comprises an n-type dopant such as phosphorous or arsenic. Alternatively, the ion beam C can include a p-type dopant in an embodiment that uses an n-type pre-doped material 202 for the silicon substrate 201. The selective emitter 208 is implanted to a depth and distance from the surface 207 into the pre-doped material 202. The distance of the selective emitter 208 from the surface 207 is determined according to an amount of energy E2 used in the ion beam C. The distance also depends on a dopant concentration level chosen for the ion beam C. The amount of energy E2 can depend on the desired specifications for the solar cell device. In an alternative embodiment, the step 201B includes multiple implantations using varying energy levels and varying dopant concentration levels of the ion beam C. In one embodiment, the energy E2 can be a continuum of variability to provide a tailored atomic profile. Such profile tailoring is described in further detail in a co-pending Patent Application Serial No. XXXXXX, entitled, "Formation of Solar Cell Selective Emitter Using Implant and Anneal Method," filed June 11, 2009, which is hereby incorporated in the entirety.

An annealing step heats the silicon substrate 201 to a temperature near but well below melting and restores any damage to the crystal structure of the silicon substrate 201 caused by the ion implantation. Also, such annealing will cause activation of dopant atoms. A temperature and time of such annealing and activation can be as low as 400-500 degrees Celsius, which is a sufficient temperature to eliminate any di-vacancies (missing atoms of a

lattice structure of the silicon substrate 201) and to provide enough activation of the dopant atoms. The annealing step can comprise furnace annealing. Alternatively, a laser annealing or flash lamp annealing can be used in place of the furnace annealing. The annealing step does not adversely affect subsequent process steps described below. In an alternative
5 embodiment, the anneal step here can be eliminated until the final anneal step below (Figure 6).

A surface texturing process can be included with the step 201B implantation of the selective emitter 208. Surface texturing provides a good light capture and adherence to the surface contour and thus will improve a contact formation that is described below. The
10 selective emitter 208 can have a resistivity in the range of 10 to 40 Ohms/square. In an exemplary embodiment, the resistivity of the selective emitter 208 comprises approximately 25 Ohms/square.

The step 201C illustrates the completed selective emitter structure 205.

Figure 3, illustrates a method of making a selective emitter structure (step 301C) 305
15 using an implantation process according to yet another embodiment of the present invention. The selective emitter structure 305 is similar to the selective emitter structure 205 described above in Figure 2. At the step 301A, a silicon substrate 301 is provided that is pre-doped with a dopant 302. The silicon substrate 301 comprises a wafer of mono, poly or multi
20 crystalline silicon material. In an exemplary embodiment, the silicon substrate comprises a 156 x 156 mm wafer. Other suitable substrates known to a person of ordinary skill can also be used for the silicon substrate 301. In an exemplary embodiment, the silicon substrate 301 includes a pre-doped material 302. The pre-doped material 302 is pre-doped with a p-type
25 dopant. The pre-doped material 302 can have a resistivity in the range of 0.5-1.5 Ohms/cm and atomic concentration of less than 5×10^{16} /cm-cube. The implantation system as described above, includes a high productivity for the formation of a homogeneous lightly doped region or homogeneous layer 304. The homogeneous layer 304 is a high resistivity region. The
purpose of the homogeneous layer 304 is the formation of electron-hole pairs as the result of an incidence of light. In operation, the homogeneous layer 304 requires a relatively low level of dopant (high resistivity) to facilitate the formation of charge carriers. An ion beam A is
30 used for the implantation of the homogeneous layer 304. The ion beam A implants the homogeneous layer 304 in a blanket fashion in the pre-doped material 302. In implanting the homogeneous layer 304, either a spot beam or wide plasma beam is used to provide full coverage across the silicon substrate 301. A productivity of the implantation system comprises approximately 1000 or more wafers per hour.

A p-n junction 303 is formed where the pre-doped material 302 and the homogeneous layer 304 meet. The junction 303 can be formed a predetermined distance from a surface 307 of the silicon substrate 301. The distance of the junction 303 from the surface 307 is determined according to an amount of energy E1 used in the ion beam A. The amount of energy E1 can be in the range of 1 to 150 KeV depending on the desired specifications for the solar cell device. The homogeneous layer 304 can have a resistivity in the range of 80 to 160 Ohms/square. In an exemplary embodiment, the resistivity of the homogeneous layer 304 comprises approximately 100 Ohms/square. An anneal step can be performed here. Alternatively, the anneal step here can be eliminated until the final anneal step below (Figure 6).

At the step 301B an ion implantation beam 'D' is used to facilitate implantation of the selective emitter 308. A registration mark or fiducial markers can be scribed onto the silicon substrate 301 using the implantation system. The registration mark can be used for alignment during the implantation process of the selective emitter 308 shown below in the step 301B.

Still referring to the step 301B, the ion implantation beam D for implanting a heavily doped region or the selective emitter 308 is shown. The ion beam D can be applied in a targeted fashion by shaping the ion beam D using a magnetic means, an electrostatic means or a combination of these means. The ion beam D can be shape to a prescribed size coinciding with a width 309 of the selective emitter 308. The ion beam D can be narrowed in one or both directions coinciding with a length and a width of the silicon substrate 301. The ion beam D can be narrowed in one direction and scanned across the length of the silicon substrate 301. Alternatively, the ion beam D can be elongated or fast scanned along the width of the silicon substrate 301. In another embodiment, the ion beam D can be formed in a top hat shaped beam during the implantation of the selective emitter 308. Using the shaped beam can help reduce dopant usage and increase the implantation process productivity. In an exemplary embodiment, the ion beam D can comprise a broad shaped ion beam. In an exemplary embodiment, the ion beam D can comprise a shaped beam or a scanning beam without any masking to generate regions of high and low dopant by manipulation of the beam, manipulation of the wafer position or by beam pulsing. Using the shaped or scanning beam without any masking provides an additive and over lapping spread of the ion beam D.

The ion beam D implants the selective emitter 308 in the homogeneous layer 304 at predetermined locations on the surface 307 of the silicon substrate 301. The ion beam D can be shaped to provide the selective emitter 308 as large as approximately 200 microns wide. Alternately, the ion beam D can be shaped to provide the selective emitter 308 as small as 50
5 microns wide. A distance or pitch 311 between each selective emitter 308 can be in the range of approximately 1 mm to 3 mm.

The ion beam D includes a dopant that is chosen depending on the manufacturer specifications. In an exemplary embodiment, the dopant for the selective emitter 308 comprises an n-type dopant such as phosphorous or arsenic. Alternatively, the ion beam D
10 can include a p-type dopant, such as Boron, in an embodiment that uses an n-type pre-doped material 302 for the silicon substrate 301. The selective emitter 308 is implanted to a depth and distance from the surface 307 into the pre-doped material 302. The distance of the selective emitter 308 from the surface 307 is determined according to an amount of energy E2 used in the ion beam D. The distance also depends on a dopant concentration level
15 chosen for the ion beam D. The amount of energy E2 can depend on the desired specifications for the solar cell device. In an alternative embodiment, the step 301B includes multiple implantations using varying energy levels and varying dopant concentration levels of the ion beam D. In one embodiment, the energy E2 can be a continuum of variability to provide a tailored atomic profile. Such profile tailoring is described in further detail in a
20 co-pending Patent Application Serial No. XXXXXX, entitled, "Formation of Solar Cell Selective Emitter Using Implant and Anneal Method," filed June 11, 2009, which is hereby incorporated in the entirety.

An annealing step heats the silicon substrate 301 to a temperature near but well below melting and restores any damage to the crystal structure of the silicon substrate 301 caused
25 by the ion implantation. Also, such annealing will cause activation of dopant atoms. A temperature and time of such annealing and activation can be as low as 400-500 degrees Celsius, which is a sufficient temperature to eliminate any di-vacancies (missing atoms of a lattice structure of the silicon substrate 301) and to provide enough activation of the dopant atoms. The annealing step can comprise furnace annealing. Alternatively, a laser annealing
30 or flash lamp annealing can be used in place of the furnace annealing. The annealing step does not adversely affect subsequent process steps described below. In an alternative embodiment, the anneal step here can be eliminated until the final anneal step below (Figure 6).

A surface texturing process can be included with the step 301B implantation of the selective emitter 308. Surface texturing provides a good light capture and adherence to the surface contour and thus will improve a contact formation that is described below. The selective emitter 308 can have a resistivity in the range of 10 to 40 Ohms/square. In an exemplary embodiment, the resistivity of the selective emitter 308 comprises approximately 25 Ohms/square.

The step 301C illustrates the completed selective emitter structure 305. The step 301D illustrates an alternative embodiment of the completed selective emitter structure 305A. The selective emitter structure 305A is similar to the completed selective emitter structure 305 except the selective emitter structure 305A includes a selective emitter 308A.

Figure 4 illustrates the formation of a transition or a seed layer 312 according to an embodiment of the present invention. A contact mask 310 is formed on the selective emitter structure 305 similarly as described above in Figure 1. The contact mask 310 is formed on the surface of the selective emitter structure 305. The contact mask 310 can be any suitable mask as known to a person of ordinary skill. Examples of such masks can include anti-reflective coverings, a nitride layer, an oxide layer, a screen-printing or any other suitable film. The contact mask 310 can be formed using processes known to a person of ordinary skill. In one embodiment, a lithography or contact printing process can be used to form the contact mask 310. A physical mask similar to the hard mask 206 (Figure 2) can also be employed.

An ion beam 'E' is used to implant the seed layer 312 over the selective emitter 308. The ion beam E can comprise a relatively high dose of metal. The arrangement of the ion beam E can be similar to those described above. The ion beam E can comprise a shaped ion beam similarly as described above. The seed layer 312 can comprise a silicide layer. The seed layer 312 can comprise various metal implantations like, Ni, Ta, Ti, W or Cu. In an exemplary embodiment, the seed layer 312 can comprise one or more layers each of a different material. The seed layer 312 alters a work function of a metal/semiconductor interface between the contact 314 (Figure 5) and the selective emitter 308. In an exemplary embodiment, the work function of the seed layer 312 is intermediate of a work function of the selective emitter 308 and a work function of the contact 314 (Figure 5). Such work function or band gap engineering can improve the metal/semiconductor interface of the contact and improve the overall performance of the solar cell 600 (Figure 6). In an exemplary embodiment, the seed layer 312 is implanted to comprise a width that is slightly smaller than the width of the selective emitter 308. The slightly smaller width of the seed layer 312 allows the lessening of contact leakage and allows the formation of a Schottky

diode. Metal-to-semiconductor contacts are of great importance since they are present in every photovoltaic device. They can behave either as a Schottky barrier or as an ohmic contact dependent on the characteristics of the metal/semiconductor interface. The control and management of the metal/semiconductor interface is of great benefit in improving the performance of the solar cell 600 (Figure 6).

Figure 5 illustrates the formation of the contact layer or contact 314 according to an embodiment of the present invention. The contact 314 is formed using a suitable metal material. The contact 314 can be formed using any well known metal deposition technique, screen printing technique or plating technique.

An annealing step heats the silicon substrate 301 to a temperature near but well below melting and restores any damage to the crystal structure of the silicon substrate 301 caused by the ion implantation and contact formation. Also, such annealing will cause activation of dopant atoms. A temperature and time of such annealing and activation can be as low as 400-500 degrees Celsius, which is a sufficient temperature to eliminate any di-vacancies (missing atoms of a lattice structure of the silicon substrate 301) and to provide enough activation of the dopant atoms. The annealing step can comprise furnace annealing. Alternatively, a laser annealing or flash lamp annealing can be used in place of the furnace annealing. The annealing step does not adversely affect subsequent process steps described below. In an alternative embodiment, the anneal step here can be eliminated until the final anneal step below (Figure 6).

Figure 6 illustrates a solar cell 600 according to an embodiment of the present invention. The contact mask 310 (Figure 5) is removed such as by chemical stripping or can be ashing. In an exemplary embodiment, a solution of NaOH (<3 wt%) or KOH (<3 wt%) is used for stripping the contact mask 310 with a spray of 2.4 bar of pressure at a dwell time of a few seconds at 55 degrees Celsius. A person of ordinary skill will appreciate other suitable solutions for stripping the contact mask 310. An anti-reflective coating (ARC) or ARC film 318 can be formed over the exposed surface 307 of the silicon substrate 301. The ARC film 318 can also be used for passivation of the homogeneous layer 304. The ARC film 318 also acts as an anti-reflective film to increase the trapping of the incident light within the solar cell 600. Thus, the ARC film 318 can improve the efficiency of the solar cell 600. A simple roller system using a dual layered organic film, such as Dupont MM500 or Shell SU8 and

other alternatives can be laminated on the surface 307. The adhesion and continuity of the ARC film 318 is critical at this lamination stage. The lamination stage is conducted at a low temperature of approximately 50-100 degrees Celsius. In an exemplary embodiment, rollers of the roller system are preheated and operated at a speed of 1 to 2 mm/min to ensure the silicon substrate 301 preferably does not reach temperatures above approximately 50 degrees Celsius.

In an alternative embodiment, the ARC film 318 can be formed using an ion implantation beam similar as described above. The ARC film 318 can be formed on the surface 307 of the silicon substrate 301 above the homogeneous layer 304. In an alternative embodiment, the ARC film 318 can be formed prior to forming the homogeneous layer 304 of the step 301A of Figure 3. The quality of the ARC film 318 is not adversely affected by the lightly doping of the homogeneous layer 304. A final anneal step similar as such annealing described above can be performed. In an exemplary embodiment, only the final anneal step is performed instead of using multiple anneal steps after each implantation as describe above.

The solar cell 600 comprises a highly efficient light conversion efficiency in between the gridlines or contacts 314. The solar cell 600 also provides a highly conductive selective emitter 308 underneath the contacts 314 and thus provide efficiency gains in the order of 1 to 2 absolute percentage points over solar cells absent of the selective emitter 308 described herein.

Figure 7 illustrates a solar cell 700 according to an alternative embodiment of the present invention. The solar cell 700 includes a pre-doped material 702 and a homogeneous layer 704. The solar cell 700 comprises a selective emitter structure 705 similar to the selective emitter structure 305A (Figure 3) described above. The selective emitter structure 705 includes the selective emitter 708. A contact 714 is formed using ion implantation using a suitable metal material. The contact 714 can be formed using ion beam epitaxy or any well known metal deposition technique as described above. In an alternative embodiment, the solar cell 700 can include an anti-reflective coating (ARC) or ARC film (not shown) formed over the exposed surface 707 of the homogeneous layer 704. Thus, the charge carriers are advantageously coupled to the contact 714 of the solar cell 700.

Figure 7A illustrates a solar cell 700A according to still another embodiment of the present invention. A selective emitter 708A can be significantly wider than the contact 714 as shown in Figure 7A. The selective emitter 708A advantageously reduces the potential of electrical leakage from the contact 714 to other areas of the solar cell 700A. The width of the selective emitter 708A can be increased by adjusting the dimensions of the ion beam D

described above (Figure 3). Further, the width of the selective emitter 708A can be increased by adjusting the dimensions of the contact mask 106 or the hard mask 201 described above in Figure 1 and Figure 2, respectively.

Turning to Figure 8, with reference to Figure 1 to Figure 7A, a process flow diagram 800 is shown for a method of forming a solar cell device 600 in accordance with an embodiment of the invention. The method begins at the step 810. A silicon substrate 101 is provided that is pre-doped with a dopant 102. In an exemplary embodiment, the dopant 102 comprises a p-type dopant. At the step 820, an implantation system is used for the formation of a homogeneous layer 104. The homogeneous layer 104 comprises a high resistivity region. An ion beam A is used for the implantation of the homogeneous layer 104. The ion beam A implants the homogeneous layer 104 in a blanket fashion in the pre-doped material 102. In implanting the homogeneous layer 104, either a spot beam or wide plasma beam is used to provide full coverage across the silicon substrate 101. A productivity of the implantation system comprises approximately 1000 or more wafers per hour. The homogeneous layer 104 can have a resistivity in the range of 80 to 160 Ohms/square. In an exemplary embodiment, the resistivity of the homogeneous layer 104 comprises approximately 100 Ohms/square. An anneal step can be performed. Alternatively, the anneal step can be eliminated.

At the step 830, a heavily doped or selective emitter 108 (Figure 1) is implanted within the lightly doped homogeneous layer 104. The selective emitter 108 is implanted in predetermined locations on the silicon substrate 101. In an exemplary embodiment, a contact mask 106 is used to facilitate the implantation of the selective emitter 108 using an ion implantation beam A in a blanket fashion. In an alternative embodiment, the selective emitter 208 (Figure 2) is implanted using a hard mask 206 and a shaped ion implantation beam C. In still another embodiment, the selective emitter 308 (Figure 3) is implanted using the shaped ion implantation beam D in a targeted fashion. A registration mark can be used for alignment of the shaped ion implantation beam D during the implantation process of the selective emitter 308. The implanted selective emitter 308 can be approximately 200 microns wide. Alternately, the selective emitter 308 can be formed approximately 50 microns wide. A distance or pitch 311 between each selective emitter 308 can be in the range of approximately 1 mm to 3 mm. The selective emitter 308 can have a resistivity in the range of 10 to 40 Ohms/square. In an exemplary embodiment, the resistivity of the selective emitter 308 comprises approximately 25 Ohms/square. An anneal step can be performed. Alternatively, the anneal step can be eliminated.

At the step 840, the seed layer 312 (Figure 4) is formed according to an embodiment of the present invention. A contact mask 310 is formed on the surface of the selective emitter structure 305. In one embodiment, a lithography or contact printing process can be used to form the contact mask 310. An ion beam E is used to implant the seed layer 312 over the selective emitter 308. The ion beam E can comprise a relatively high dose of metal. The ion beam E can comprise a shaped ion beam similarly as those described above. The seed layer 312 can comprise a silicide layer. The seed layer 312 can comprise various metal implantations like, Ni, Ta, Ti, W or Cu. In an exemplary embodiment, the seed layer 312 is implanted to comprise a width that is slightly smaller than the width of the selective emitter 308. The slightly smaller width of the seed layer 312 allows the lessening of contact leakage and allows the formation of a Schottky diode.

At the step 850, a contact 314 (Figure 5) is formed according to an embodiment of the present invention. The contact 314 is formed using ion implantation using a suitable metal material. The contact 314 can be formed using ion beam implantation similarly as described above. A dopant concentration or dopant rate similar to plasma doping can be used in forming the contact 314. Alternatively, a beamline implantation system can be used in forming the contact 314. In still another embodiment, the contact 314 can be formed using high dose rate systems such as molecular beam epitaxy, molecular beam implantation or plasma ion implantation systems. Subsequent to implantation of the contact 314, an additional implantation step of a much higher implantation concentration of similar or matched work function of the contact 314 can be used to further form the contact 314. Alternatively, a subsequent deposition step can be used on the contact 314. In still another embodiment, a subsequent ink jet spray step can be used in further forming the contact 314.

An annealing step heats the silicon substrate 301 to a temperature near but well below melting and restores any damage to the crystal structure of the silicon substrate 301 caused by the ion implantation and contact formation. Also, such annealing will cause activation of dopant atoms. A temperature and time of such annealing and activation can be as low as 400-500 degrees Celsius, which is a sufficient temperature to eliminate any di-vacancies (missing atoms of a lattice structure of the silicon substrate 301) and to provide enough activation of the dopant atoms. The annealing step can comprise furnace annealing. Alternatively, a laser annealing or flash lamp annealing can be used in place of the furnace annealing. The annealing step does not adversely affect subsequent process steps described below. In an exemplary embodiment, only a final anneal step is performed instead of using multiple anneal steps after each implantation as describe above.

A completed solar cell 600 (Figure 6) according to the method 800 is provided. The solar cell 600 includes an anti-reflective coating (ARC) or ARC film 318 formed over the exposed surface 307 of the silicon substrate 301. The ARC film 318 can be used for passivation of the homogeneous layer 304. The ARC film 318 also acts as an anti-reflective film to increase the incidence of light trapped within the solar cell 600. Thus, the ARC film 318 can improve the efficiency of the solar cell 600. The solar cell 600 comprises a highly efficient light conversion efficiency in between the gridlines or contacts 314. The solar cell 600 also provides a highly conductive selective emitter 308 underneath the contacts and thus provide efficiency gains in the order of 1 to 2 absolute percentage points over solar cells absent of the selective emitter 308 described herein. The method 800 ends at the step 860.

While the invention has been described with reference to numerous specific details, one of ordinary skill in the art will recognize that the invention can be embodied in other specific forms without departing from the spirit of the invention. Thus, one of ordinary skill in the art will understand that the invention is not to be limited by the foregoing illustrative details, but rather is to be defined by the appended claims.

CLAIMS

What is claimed is:

1. A solar cell device comprising:
a silicon substrate including a preexisting dopant included therein;
a homogeneous lightly doped region formed on a surface of the silicon substrate over the preexisting dopant, thereby forming a junction between the preexisting dopant and the lightly doped region;
a heavily doped selectively implanted region on the surface of the silicon substrate within the lightly doped region;
a seed layer formed over the heavily doped region; and
a metal contact formed over the seed layer.
2. The device of claim 1, wherein the homogenous lightly doped region is uniformly implanted.
3. The device of claim 1, further comprising an anti-reflective coating on top of the lightly doped region.
4. The device of claim 1, wherein the homogeneous lightly doped region comprises a resistivity in a range of 80 to 160 Ohms/square.
5. The device of claim 4, wherein the homogeneous lightly doped region comprises a resistivity approximately 100 Ohms/square.
6. The device of claim 1, wherein the heavily doped region comprises a resistivity in a range of 10 to 40 Ohms/square.
7. The device of claim 6, wherein the heavily doped region comprises a resistivity approximately 25 Ohms/square.
8. The device of claim 1, wherein the junction is formed a predetermined distance from the surface of the silicon substrate.
9. The device of claim 1, wherein the seed layer comprises a silicide.

10. The device of claim 1, wherein the seed layer is formed by implanting a material from the group consisting of one or more of Ni, Ta, Ti, W or Cu.
11. The device of claim 1, wherein the heavily doped regions each comprise a width on the silicon substrate a distance in the range 50 to 200 microns.
12. The device of claim 1, wherein the heavily doped regions are laterally spaced on the silicon substrate a distance in the range 1 to 3 mm from each other.
13. The device of claim 1, wherein the silicon substrate includes fiducial markers configured for aligning the placement of the heavily doped regions during an ion implantation process.
14. A method of forming a solar cell device comprising the steps of:
providing a silicon substrate including a preexisting dopant included therein;
using an ion implantation process to form a homogeneous lightly doped region on a surface of the silicon substrate over the preexisting dopant, thereby forming a junction between the preexisting dopant and the lightly doped region;
using a selective ion implantation process to form a heavily doped region implanted on the surface of the silicon substrate within the lightly doped region, the heavily doped region being implanted at predetermined locations on the silicon substrate surface;
using the selective ion implantation process to form a seed layer over the heavily doped region; and
using the selective ion implantation process to form a metal contact over the seed layer.
15. The method of claim 14, further comprising using the selective ion implantation process to form an anti-reflective coating.
16. The method of claim 14, wherein the heavily doped region is implanted at predetermined locations on the silicon substrate surface using a physical mask, the physical mask having openings aligned with the predetermined locations.

17. The method of claim 16, wherein the physical mask is formed on the surface of the silicon substrate.
18. The method of claim 16, wherein the physical mask is positioned a predetermined distance above the surface of the silicon substrate during the selective ion implantation process to form the heavily doped region.
19. The method of claim 14, wherein the selective ion implantation process uses a shaped ion beam that is aligned with the predetermined locations to form the heavily doped region.
20. The method of claim 14, wherein the homogeneous lightly doped region comprises a resistivity in a range of 80 to 160 Ohms/square.
21. The method of claim 20, wherein the homogeneous lightly doped region comprises a resistivity approximately 100 Ohms/square.
22. The method of claim 14, wherein the heavily doped region comprises a resistivity in a range of 10 to 40 Ohms/square.
23. The method of claim 22, wherein the heavily doped region comprises a resistivity approximately 25 Ohms/square.
24. The method of claim 14, wherein the junction is formed a predetermined distance from the surface of the silicon substrate.
25. The method of claim 14, wherein the seed layer comprises a silicide.
26. The method of claim 14, wherein the seed layer comprises a layer of a material, wherein the material is Ni, Ta, Ti, W or Cu.
27. The method of claim 14, wherein the heavily doped regions each comprise a width on the silicon substrate a distance in the range 50 to 200 microns.

28. The method of claim 14, wherein the heavily doped regions are laterally spaced on the silicon substrate a distance in the range 1 to 3 mm from each other.
29. The method of claim 14, wherein the silicon substrate includes fiducial markers configured for aligning the placement of the heavily doped regions during the selective ion implantation process.
30. The method of claim 14, further comprising using an annealing process on the silicon substrate having the homogeneous lightly doped region.
31. The method of claim 14, further comprising using an annealing process on the silicon substrate after forming the metal contact.
32. A solar cell device comprising:
 - a silicon substrate including a preexisting dopant included therein;
 - a homogeneous lightly doped region formed on a surface of the silicon substrate over the preexisting dopant, thereby forming a junction between the preexisting dopant and the lightly doped region;
 - a heavily doped region selectively implanted on the surface of the silicon substrate within the lightly doped region, the heavily doped region being as a function of distance from the surface of the silicon substrate; and
 - a metal contact formed over the heavily doped region.
33. The device of claim 32, further comprising a seed layer formed over the heavily doped region and beneath the metal contact.
34. The device of claim 32, further comprising an anti-reflective coating.
35. The device of claim 32, wherein the homogeneous lightly doped region comprises a resistivity in a range of 80 to 160 Ohms/square.
36. The device of claim 35, wherein the homogeneous lightly doped region comprises a resistivity approximately 100 Ohms/square.

37. The device of claim 32, wherein the heavily doped region comprises a resistivity in a range of 10 to 40 Ohms/square.
38. The device of claim 37, wherein the heavily doped region comprises a resistivity approximately 25 Ohms/square.
39. The device of claim 32, wherein the junction is formed a predetermined distance from the surface of the silicon substrate.
40. The device of claim 32, wherein the lateral grade of the heavily doped region comprises a parabolic shape.
41. The device of claim 33, wherein the seed layer comprises a silicide.
42. The device of claim 33, wherein the seed layer comprises a layer of a material, wherein the material is Ni, Ta, Ti, W or Cu.
43. The device of claim 32, wherein the heavily doped regions each comprise a width on the silicon substrate a distance in the range 50 to 200 microns.
44. The device of claim 32, wherein the heavily doped regions are laterally spaced on the silicon substrate a distance in the range 1 to 3 mm from each other.
45. The device of claim 32, wherein the silicon substrate includes fiducial markers configured for aligning the placement of the heavily doped regions during an ion implantation process.