ABSTRACT OF THE DISCLOSURE

CASTELLATED CHIP-SCALE PACKAGES AND METHODS FOR FABRICATING THE SAME

A method for fabricating a chip-scale package includes securing a device substrate that carries at least two adjacent semiconductor devices to a sacrificial substrate. The sacrificial substrate may include conductive elements on a surface thereof, which are located so as to align along a street between each adjacent pair of semiconductor devices on the device substrate. The device substrate is then severed along each street and the newly formed peripheral edge of each semiconductor device coated with dielectric material. If the sacrificial substrate includes conductive elements, they may be exposed between adjacent semiconductor devices and subsequently serve as lower sections of contacts. Peripheral sections of contacts are formed on the peripheral edge. Upper sections of the contacts may also be formed over the active surfaces of the semiconductor devices. Once the contacts are formed, the sacrificial substrate is substantially removed from the back sides of the semiconductor devices.

[FIG. 1]