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DIGITAL SIGNAL PROCESSING CIRCUIT FOR A TELEVISION RECEIVER

The present invention relates to a digital signal processing circuit for a television receiver, which circuit supports up-conversion and digital zooming.

Zooming in this context means to expand a picture, or a portion of a picture, by adding additional lines to the picture, said lines being generated according to interpolation techniques. Zooming may, in particular, be used to convert a picture transmitted in the letterbox format, into a picture covering the whole screen.

In regard to up-conversion there are currently two, common, approaches. One is the so-called 100/120 Hz interlaced scanning approach, the other is the so-called 50/60 Hz progressive scan conversion approach.

Figures 1b and 1c illustrate the principle of these two techniques, whereas Figure 1a illustrates traditional 50/60 Hz interlaced scanning.

According to traditional 50/60 Hz interlaced scanning, every picture (frame) is divided into two fields, one field comprising the odd lines of the complete frame, the other field comprising even lines of the complete frame. The two fields A and B, forming together a full frame, are displayed at successive times, which is illustrated in Figure 1 by the field sequence A,B,A,....

The 100/120 Hz interlaced scanning technique differs from the traditional 50/60 Hz interlaced scanning in that four timely successive fields are displayed during one frame period. In the simplest form, this can be achieved by field repetition leading to field sequence of A,A,B,B,.... Such simple repetition of the fields reduces only the large area flicker, the line flicker is the same or even increased compared with a normal 50/60 Hz interlaced display. A second form is achieved by frame repetition leading to field sequence A,B,A,B,.... This method leads to acceptable results in case of pictures that are practically without motion (still picture). In order to enhance the picture quality achievable with 100/120 Hz interlaced scanning, it is proposed that motion adaptive filtering is used, in that generation of additional fields is performed, dependent on the amount of motion contained in the picture. This is illustrated in Figure 1b, by the sequence AA*,BB*....If motion is existent, fields A and B are not merely repeated, but the additional fields A*, B* are generated, dependent on the amount of motion present in the picture.

Figure 1c illustrates the 50/60 Hz progressive scanning technique. According to this technique, to each field A,B, the respective missing odd or even lines are added, so that two interlaced fields, A/A*, B*/B, are simultaneously displayed.

It is the object of the present invention to provide a digital signal processing circuit for a television receiver, which circuit combines up-conversion processing

with zooming processing, whereby the circuit may be realised using relatively simple hardware.

This object is solved by the subject matter of present claim 1.

Preferred embodiments of the present invention are the subject matter of the dependent claims to claim 1.

In the following a preferred embodiment of the present invention is described in detail, in connection with the accompanying drawings, which show:

Fig. 1a-c illustrations for describing traditional 50/60 Hz interlaced scanning, 100/120 Hz interlaced scanning and 50/60 Hz progressive scanning,

Fig. 2 a schematic diagram of a circuit combining up-conversion-, zooming- and panning-capabilities,

Fig. 3 a schematic diagram of a circuit combining motion dependent up-conversion-, zooming- and panning-capabilities, and

Figs 4 & 5 diagrams for illustrating the operation of the phase accumulation means.

The circuit according to Figure 2 basically comprises three main units, namely a field memory 1, a filter unit 2 and a control unit 3. Field memory 1, which is preferably a field RAM, stores one field of an incoming video signal,

whereby the video signal comprises only luminance or chrominance signals of the incoming video signal, or both. Filter unit 2 is preferably a so-called FIR-filter and most preferably a 2-tap FIR-filter. The filter unit comprises a line memory 4, adder means 5 and 6, and a multiplier 7. As will be understood by those skilled in the art, if filter unit 2 is a 2-tap-filter, as illustrated in Figure 2, the filter operation may be mathematically expressed as follows:

$$Y = kX_0+(1-k)X_{-1},$$

whereby X_0 represents a current line, X_{-1} represents a line succeeding the current line and y represents the output of the filter unit. Factor k is applied by control unit 3 and, as is apparent from the above formula, determines the ratio by which a current line and the adjacent succeeding line are mixed to provide an interpolated line.

If there is no zooming, no additional lines to the lines already stored in field memory have to be generated, and so factor k can be selected with a value of 0 in order not to change the lines provided by field memory 1. If there is zooming the generation of additional lines is necessary. For example, to expand a picture received in the letterbox format, to a format matching the full size of the screen, it is necessary to generate additional lines by interpolating lines adjacent to the active part of the picture.

Control unit 3 is preferably a so-called phase accumulator unit, basically comprising a line address counter 8, an

adder means 9 and a delay or register means 10. Since control unit 3 addresses, via line address counter 8, field memory 1, and simultaneously supplies factor k to multiplier 7 of filter unit 2, it controls which of the lines stored in field memory 1 are interpolated with each other, and according to which ratio.

As shown in Figure 2, controller unit 3 preferably comprises adder means 9 receiving at a first input an initial value or a zoom factor and, at a second input, the low 6 bits (0..5) output of register means 10. Register means 10 coupled to the output of the adder means 9 delays the input from adder means 9 by a time period corresponding to one line. Adder means 9 is preferably a seven bit adder and thus provides a seven bit word to register means 10. The seven bit output from register means 10 is split, in that the most significant bit is applied to line address counter 8, and the lower 6 bits (0..5) are applied to multiplier 7, of filter unit 2. These lower 6 bits are also applied to one of the inputs of the adder.

The phase accumulation means 3 is executed every output line. The physical distance between two lines of the input field is divided into 64 steps. Theoretically it is possible to generate at every step position an output line by interpolation. If a zooming factor from one to two is realised then, at maximum, two of these new interpolated output lines are required. Therefore, there is no need to generate a line at all 64 steps.

The output of control unit means 3 can be described by the following mathematical formulae:

k_0 = INIT mod 64

k_n = (k_{n-1} + comp) mod 64 (n = 1,2,3,...)

la_0 = INIT div 64

la_n = la_n + (k_{n-1} + comp) div 64 (n = 1,2,3,...)

where: INIT = initial value, which depends on the field (A1,A1*,B1* or B1) generated

k = value given to multiplier means 7 (bit 0..5)

k_0 = k-factor for the first output line (line No. 0)

la = output of line address counter

n = output line number to be generated (n = 1,2...)

comp = compression factor (32...64)

mod = modulo operation (rest of division)

div = division operation (integer result of division)

The following example illustrates the above given formulae:

The output field is A1 and the compression factor is 50. This means that only 78% of the incoming picture is displayed (50/64 = 0.78; with an initial value for A1=64). In Figure 4, the generation of output field A1 with n=0 and n=1 is shown.

n	k_n	1-k_n	la=output line of Field Memory	Output line of Line Memory
0	0	64	1	0
1	50	14	1	0
2	36	28	2	1
3	22	42	3	2
4	8	56	4	3
5	58	6	4	3
6	44	20	5	4
...	...	...	...	...

The output field is A1* and the compression factor is 50. For output field A1* the initial value is (64 + comp/2) = 89.

n	k_n	$1-k_n$	la=output line of Field Memory	Output line of Line Memory
0	25	39	1	0
1	11	53	2	1
2	61	3	2	1
3	47	17	3	2
4	33	31	4	3
5	19	45	5	4
6	5	59	6	5
...	...	...	...	...

Figure 3 geometrically indicates a preferred embodiment of a circuit according to the present invention, combining motion adaptive up-conversion-, zooming- and panning-capabilities.

The circuit shown in Figure 3 comprises a field memory 1' and a filter unit 2', which basically provide the same function as units 1 and 2 of Figure 2. Unit 2 is preferably the 2-tap FIR-filter for intra-field interpolation, which result is used in case of motion. The circuit of Figure 3 further comprises a control unit 11 controlling the addressing of field memory 1' and filter unit 2', similar to control unit 3 in Figure 2. The circuit of Figure 3 additionally comprises a further field memory 12 and a further filter unit 13.

Unit 13 is preferably a 3-tap FIR-filter for intra-frame interpolation, which is used in case of no motion or slow motion. Preferably one coefficient of the 3-tap filter is always set to zero. Therefore, the 3-tap filter can be

realised by a 2-tap FIR-filter with multiplexers means 17 and 18, which are described below.

Briefly explained, filter unit 13 performs a similar filter operation to that of filter unit 2' based however, on different input signals. Control unit 11 controls both, filter unit 2' and filter unit 13.

Mixer unit 14 combines the output of filter unit 2' and the output of filter unit 13 and outputs, through normalisation unit 19, the resultant video signal. The operation of mixer unit 14 is controlled by a motion signal supplied from a motion detection unit (not shown).

Basically, mixer 14 passes the output from filter unit 13 to its output if there is no motion, and passes the output signal from filter unit 2' to its output if there is maximum motion. In the case of intermediate motion values, mixer 14 combines the outputs of filter units 2' and 13.

As shown in Figure 3, control unit 11 applies a control signal to filter unit 2' and filter unit 13. These control signals are preferably supplied to multiplier 15 and multiplier 16 respectively.

The phase accumulation means 11 is executed for every output line. The physical distance between two lines of the output field is divided into 128 steps. Theoretically, it is possible to generate at every step position an output line by interpolation. If a zooming factor from one to two is realised then, at maximum, in 100/120 Hz mode two, and in 50/60 Hz mode, four of these new interpolated output

lines are required. Therefore, there is no need to generate a line at all 128 steps.

The output of control unit means 11 can be described by the following mathematical formulae:

6 Bit Adder and Reg:

$$km_0 = INIT/2 \bmod 64$$
$$km_n = (k_{n-1} + comp/2) \bmod 64 \quad (n = 1,2,3,...)$$

8 Bit Adder and Reg:

$$temp_0 = INIT \bmod 128$$
$$temp_n = (temp_{n-1} + comp) \bmod 128 \quad (n = 1,2,3,...)$$
$$knm_n = temp_n \bmod 64 \quad (n = 0,1,2,3,...)$$
$$mux_n = temp_n \text{ div } 64 \quad (n = 0,1,2,3,...)$$
$$la_0 = INIT \text{ div } 128$$
$$la_n = la_{n-1} + (k_{n-1} + comp) \text{ div } 128 \quad (n = 1,2,3,..)$$

where: INIT = initial value, which depends on the field to be generated (A1,A1*,B1* or B1)
km = value given to multiplier means 15 (bit 0..5)
km_0 = k-factor for multiplier means 15 of the first output line

temp = temporal variable
knm = value given to multiplier means 16 (bit 0..5)
mux = mux_ctrl, signal to control multiplexers means 17 and 18
la = output of line address counter
n = output line number to be generated (n=0,1,2..)

comp = compression factor (64,68,72...128)
mod = modulo operation (rest of division)
div = division operation (integer result of division)

The output of the line address counter is given to the field memory means 1. The address, which is given to field memory means 12 can differ by one line, dependent of the field (A1,A1*,B1* or B1) to be generated.

The two multiplexers (17, 18) are controlled by a mux_ctrl signal. If the mux_ctrl signal is "0" then the output of the line memory means 2 and the output of the field memory means 12 is applied to the filter means 13. If the mux_ctrl signal is "1" then the output of the field memory means 1 and the output of the line memory means 2 is applied to the filter means 13.

The following example may illustrate the above given formulae.

If output field is A1 and the compression factor is 100, only 78% of the incoming picture is displayed (since 100/64 = 0.78 with an initial value for A1 = 128)

n	km_n	64-km_n	$temp_n$	knm_n	64-knm_n	mux_n	l_n = output line of Field Memory means 1	Output line of Line Memory means 2	Output line of Field Memory means 12
0	0	64	0	0	64	0	1	0	0
1	50	14	100	36	28	1	1	0	0
2	36	28	72	8	56	1	2	1	1
3	22	42	44	44	29	0	3	2	2
4	8	56	16	16	48	0	4	3	3
5	58	6	116	52	12	1	4	3	3
6	44	20	88	24	40	1	5	4	4
...	...	...	...	...	...	...	...	...	...

The output field is A1* and the compression factor is 100.

For output field A1* the initial value is (128+comp/2)=178.

n	km_n	64-km_n	$temp_n$	knm_n	64-knm_n	mux_0	la = output line of Field Memory means 1	Output line of Line Memory means 2	Output line of Field Memory means 12
0	25	39	50	50	14	0	1	0	0
1	11	53	22	22	42	0	2	1	1
2	61	3	122	58	6	1	2	1	1
3	47	17	94	30	34	1	3	2	2
4	33	31	66	2	62	1	4	3	3
5	19	45	38	38	26	0	5	3	3
6	5	59	10	10	54	0	6	4	4
...	...	...	...	...	...	...	...	...	...

Figure 5 illustrates the generation of output field A1 with n=0 and n=1. In the second column the output of the 2-tap filter means is shown and in the third column the output of the 3-tap filter means 13 is shown.

As mentioned, the circuit according to Figure 3 combines up-conversion capabilities with zooming and panning capabilities. Thereby the circuit according to Fig. 3 is able to perform interlaced scan conversion and progressive scan conversion.

The principle operation of the circuit shown in Figure 3 for different situations, i.e. as interlaced scanning or progressive scanning, zooming or no zooming, motion or no motion (still), will be explained in connection with the following Tables 1 and 2.

incoming video fields	B0	A1		B1		A2
output video fields		A1	A1*	B1*	B1	A2
used data for interpolation in case of:						
1. no zoom and motion		A1	A1, A1 LD	B1, B1LD	B1	
2. no zoom and still		A1	B0	A1	B1	
3. zoom and motion		A1, A1LD	A1, A1LD	B1, B1LD	B1, B1LD	
4. zoom and still		A1, A1LD, B0	A1, A1LD, B0	A1, B1, B1LD	A1, B1, B1LD	

LD: line delay
this is for a geometical offset

Table 1: incoming video data for 120 / 100 Hz interlaced scan conversion

incoming video fields	B0	A1	B1	A2
output video fields		A1 / A1*	B1* / B1	A2 / A2*
used data for interpolation in case of:				
1. no zoom and motion		A1, A1LD	B1, B1LD	
2. no zoom and still		A1, B0	A1, B1	
3. zoom and motion		A1, A1LD	B1, B1LD	
4. zoom and still		A1, A1LD, B0	A1, B1, B1LD	

LD: line delay
this is for a geometical offset

Table 2: incoming video data for 50 / 60 Hz progressive scan conversion

Table 1 concerns the operation of the circuit with regard to interlaced scanning and in particular for 100/120 Hz interlaced scan conversion.

As mentioned above, in the case of interlace scanning, the amount of fields is doubled, in that during the time period of a field A1 of an incoming video signal, two fields A1, A1* are generated and displayed.

In the case of no zooming and no motion (still) in the picture, sub-field A1 is identical to incoming field A1 and sub-field A1* is identical to the previous incoming field BO (situation 2).

In the case of no zooming, but with motion, sub-field A1 is identical to incoming field A1, the lines of sub-field A1* are however, generated by interpolating adjacent lines of incoming field A1. This is indicated in Table 1 by the expression A1,A1LD, whereby LD designates "line delay" (situation 1).

In the case of zooming and motion, the lines of both sub-fields A1 and A1* are generated by interpolating respective adjacent lines of incoming field A1 (situation 3).

In the final case of Table 1, a situation with zooming and no motion (still) (situation 4), lines of sub-fields A1 and A1* are generated by interpolating adjacent lines of incoming field A1 and lines of previous field B0. Although explained in more detail herein below, it should be mentioned that interpolation between lines of adjacent

incoming fields A1 and B0 is achieved by the operation of multiplexer 17 and 18 of filter unit 13.

Table 2 illustrates the situation in the case of progressive scan conversion. As mentioned above, in the case of progressive scan conversion, each incoming field is, by interpolation, expanded into a frame whereby all lines of the resultant frame are displayed during the same field period.

Table 2 shows the manner in which individual lines of frames A1/A1* and B1*/B1 are generated for the mentioned four different situations.

In case of 100/120 Hz interlaced scan conversion and output field A1 and A1*, the output data of field memory means 1 is data of input field A1 and the output data of the line memory means 2 is input field A1 one line delayed. The output of field memory means 12 is the input field B0. Thus, the input of the 2-tap filter means 2 is input field A1 and input field A1 one line delayed (A1LD). One coefficient of the 3-tap filter is preferably always set to zero, in that it can be realised by a 2-tap filter with multiplexers.

In case of output field B1* and B1, the output data of field memory means 1 is data of input field B1 and the output data of the line memory means 2 is input field B1 one line delayed. The output of field memory means 12 is input field A1. Thus, the input of the 2-tap filter means 2 is input field B1 and input field B1 one line delayed (B1LD). The input of the 3-tap filter means 13 is input

field B1 and B1LD and the input field A1. One coefficient of the 3-tap filter is preferably always set to zero, in that it can be realised by a 2-tap filter with multiplexers.

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CLAIMS

1. Digital signal processing circuit for a television receiver comprising:

a first field memory (1; 1') for storing input data representative of the chrominance or luminance portion of one field;

first interpolation means (2; 2') for generating interpolated line data based on line data received from said first field memory;

zooming and up-conversion control means (3; 11) for controlling the read-out of line data from said first field memory and the interpolation performed by said interpolation means based on a zoom factor input to said zooming and up-conversion control means.

2. Digital signal processing circuit according to claim 1, wherein said first interpolation means is a FIR-filter, preferably a 2-tap FIR-filter.

3. Digital signal processing circuit according to claim 2, wherein said FIR-filter comprises weighting means (7) which are

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controlled by said zooming and up-conversion control means (3; 11).

4. Digital signal processing circuit according to one of the preceding claims, wherein said zooming and up-conversion control means determines the first line data to be read out from the first field memory in accordance with a received active area signal in that only relevant line data is supplied to the interpolation means.

5. Digital signal processing circuit according to one of the preceding claims, wherein said interpolation means comprises at least one line memory for outputting a one line-delayed version of the current line data output from the first field memory.

6. Digital signal processing circuit according to one of the preceding claims, wherein said zooming and up-conversion control means comprises adder means (9), line delay means (10) and line address counter means (8), wherein

said adder means receives said zoom factor as a first input and provides output data to said line delay means (10),

said line delay means (10) provides output data to said interpolation means and to said adder means as a second input thereof,

said line address counter (8) receives the MSB from the output of the line delay means and controls by its output the read-out of the first field memory.

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7. Digital signal processing circuit according to claim 5, wherein said adder means is a 7-bit adder and said line delay means provides the six lower bits of its output to the second input of the adder means and to the interpolation means and provides the most significant bit of its output to said line address counter means (8).

8. Digital signal processing circuit according to one of the claims 1-5, wherein said digital signal processor further comprises:

a second field memory (12), a second interpolation means (13) and a mixer means (14), wherein,

said second field memory is coupled to the output of the first field memory,

said second interpolation means (13) receives as a first input the output of the second field memory (12), as a second input the output of the first field memory (1') and as a third input a one-line-delayed version of the output of the first field memory and generates, based on either the first and second or the first and third inputs, interpolated line data,

said mixer means (14) receives the output data from the first and the second interpolation means (2', 13) and generates output data based on the two inputs and based on a motion signal supplied by a motion detection unit.

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9. Digital signal processing circuit according to claim 8, wherein said second interpolation means is an FIR-filter and preferably a 2-tap FIR-filter.

10. Digital signal processing circuit according to claim 9, wherein said FIR-filter comprises weighting means (16) which are controlled by said zooming and up-conversion means (3; 11).

11. Digital signal processing circuit according to claim 10, wherein said FIR-filter comprises multiplexer means (17, 18) for passing either the first and second or first and third input to the FIR-filter.

12. Digital signal processing circuit according to one of the claims 8-11, wherein said zooming and up-conversion means (11) controls the weighting operation performed within the first interpolation means and the weighting operation performed by the second interpolation means and further controls the switching of the multiplexer contained in the second interpolation means (13).

13. Digital signal processing circuit according to one of the claims 8-12, wherein the third input to the second interpolation means is provided by a line delay means comprised in the first interpolation means.

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DIGITAL SIGNAL PROCESSING CIRCUIT FOR A TELEVISION RECEIVER

ABSTRACT

Digital signal processing circuit for a television receiver comprising: a first field memory for storing input data representative of the chrominance or luminance portion of one field; first interpolation means for generating interpolated line data based on line data received from said first field memory; zooming and up-conversion control means for controlling the read-out of line data from said first field memory and the interpolation performed by said interpolation means based on a zoom factor input to said zooming and up-conversion control means.

(No suitable figure)

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Fig. 1a

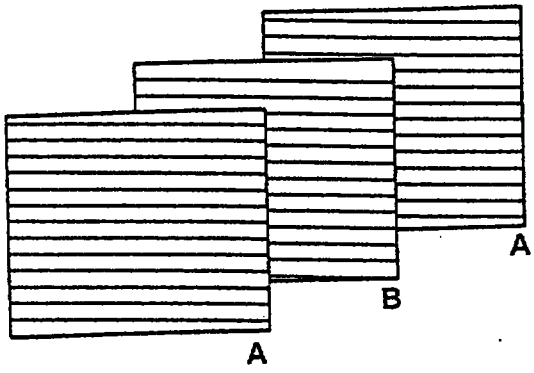


Fig. 1b

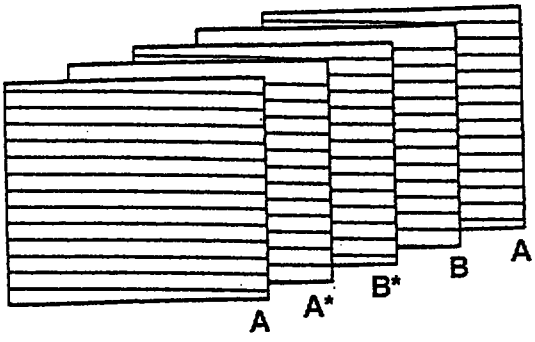
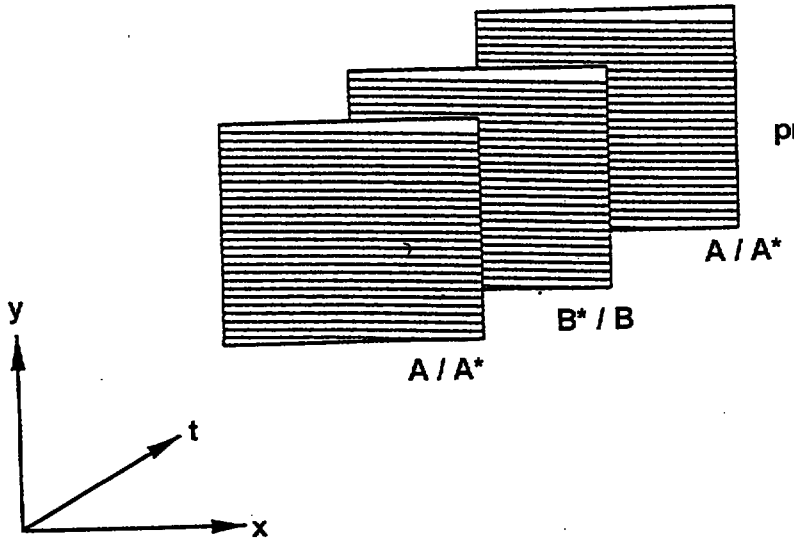


Fig. 1c



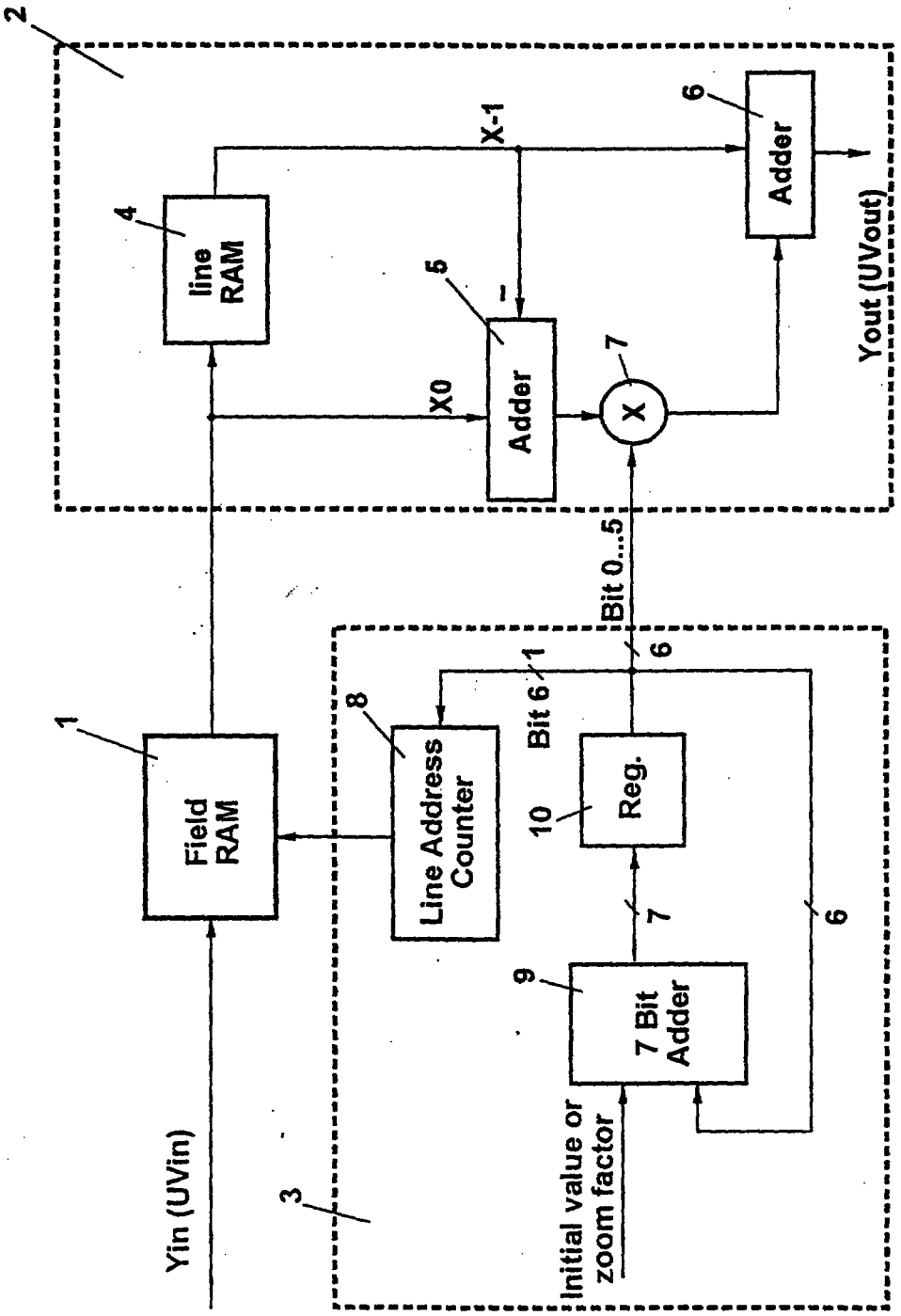

2
6
Adder
X-1
4
line RAM
5
–
Adder
X0
7
X
Yout (UVout)
Bit 0...5
1
6
8
Bit 6
Line Address Counter
10
Reg.
1
Field RAM
7
6
9
7 Bit Adder
Initial value or zoom factor
Yin (UVin)
3

Fig. 2

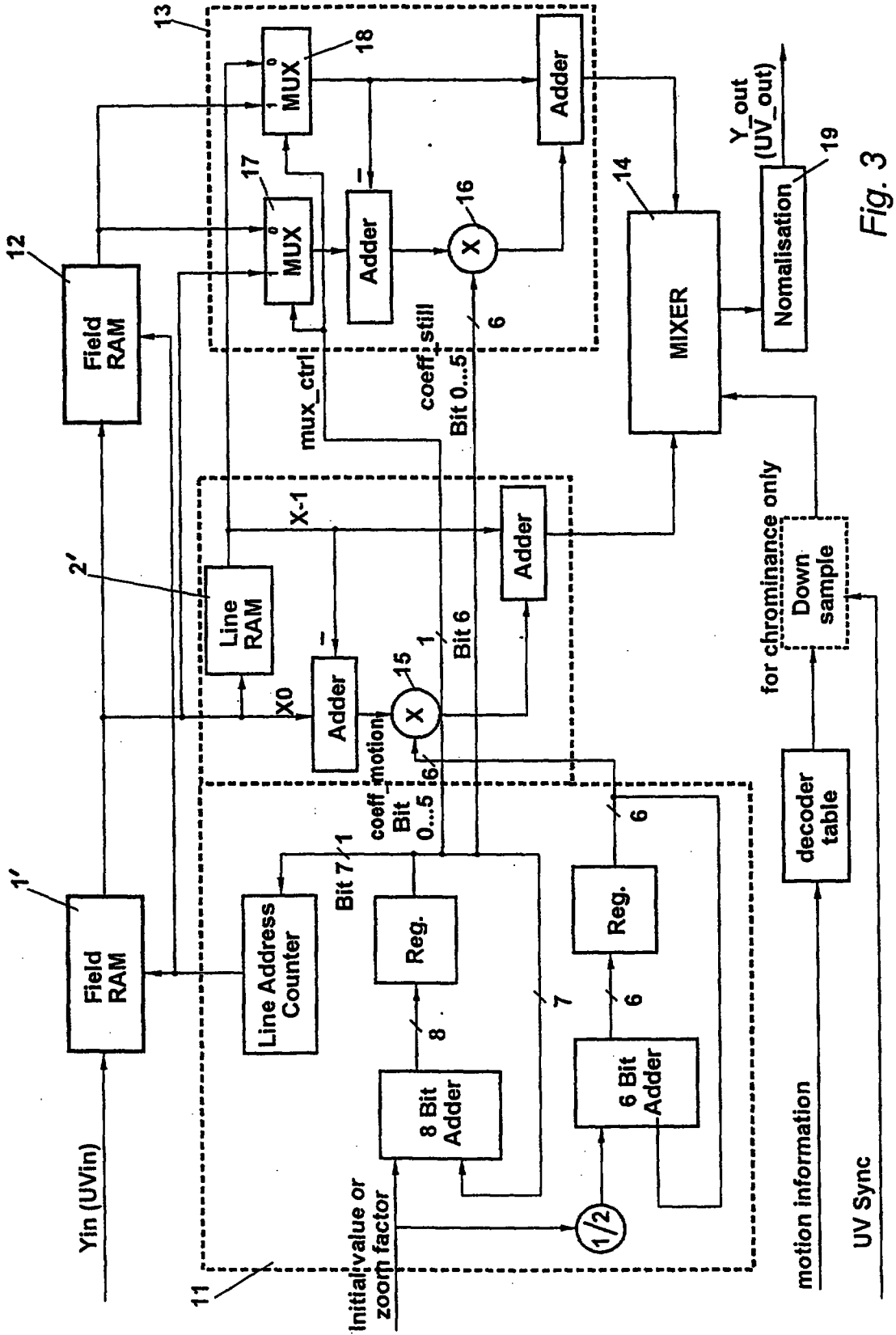

Yin (UVin)
Field RAM
1'
Line Address Counter
11
Initial value or zoom factor
8 Bit Adder
Reg.
Bit 7
1
8
coeff_motion Bit 0...5
6
7
1/2
6 Bit Adder
Reg.
6
decoder table
motion information
UV Sync
for chrominance only
Down sample
Field RAM
12
Line RAM
2'
X0
X-1
Adder
15
Bit 6
Adder
13
MUX
18
MUX
17
Adder
16
mux_ctrl
coeff_still Bit 0...5
6
Adder
MIXER
14
Nomalisation
19
Y_out (UV_out)

Fig. 3

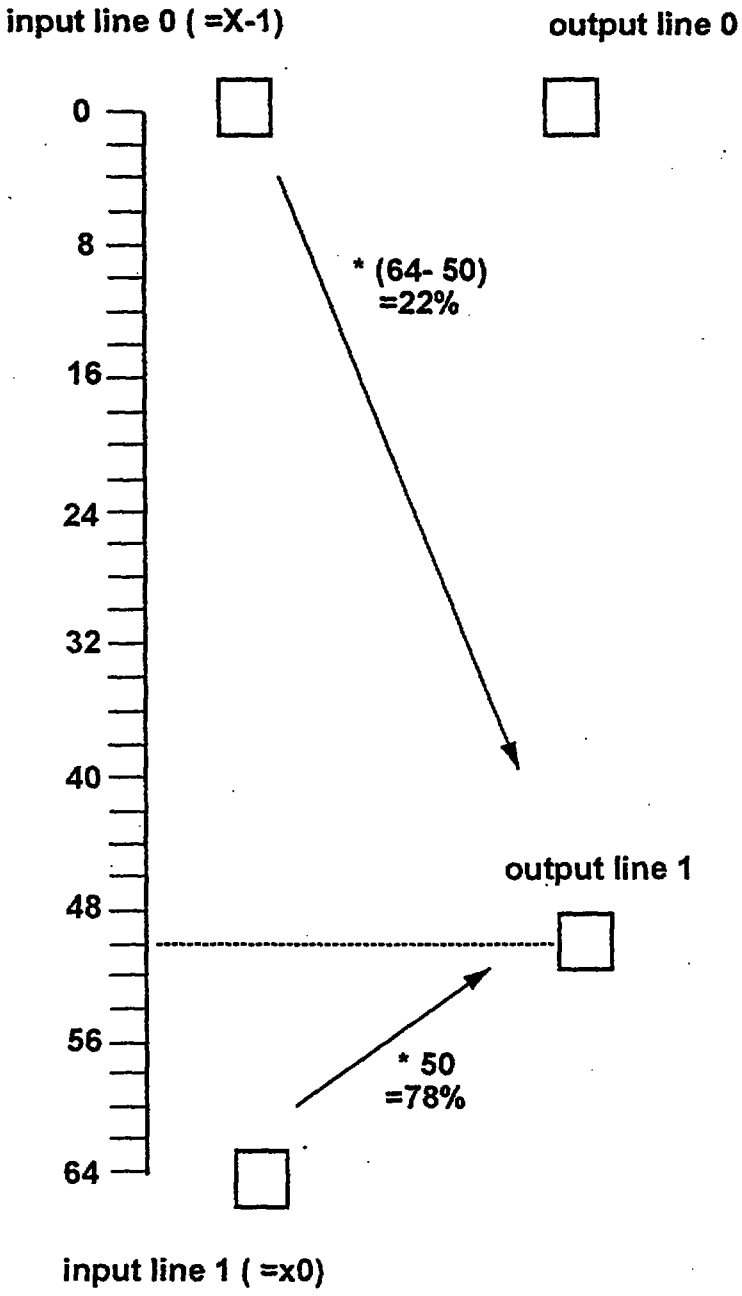

input line 0 (=X-1)
output line 0
0
8
16
24
32
40
48
56
64
* (64- 50)
=22%
output line 1
* 50
=78%
input line 1 (=x0)

Fig. 4

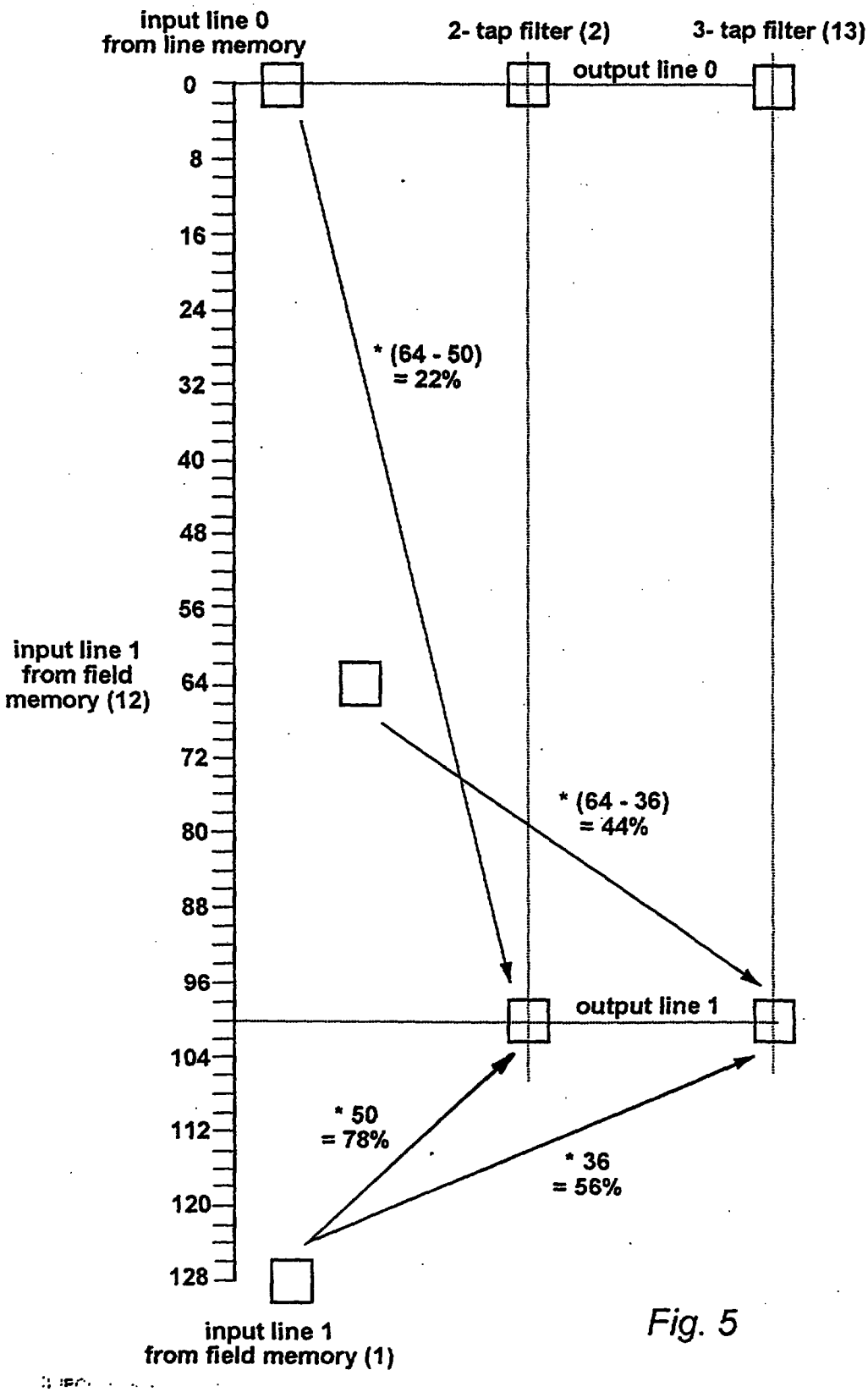

input line 0
from line memory
2- tap filter (2)
3- tap filter (13)
output line 0
0
8
16
24
32
40
48
56
64
72
80
88
96
104
112
120
128
* (64 - 50)
= 22%
input line 1
from field
memory (12)
* (64 - 36)
= 44%
output line 1
* 50
= 78%
* 36
= 56%
input line 1
from field memory (1)

Fig. 5

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controlled by said zooming and up-conversion control means (3; 11).

4. Digital signal processing circuit according to one of the preceding claims, wherein said zooming and up-conversion control means determines the first line data to be read out from the first field memory in accordance with a received active area signal in that only relevant line data is supplied to the interpolation means.

5. Digital signal processing circuit according to one of the preceding claims, wherein said interpolation means comprises at least one line memory for outputting a one line-delayed version of the current line data output from the first field memory.

6. Digital signal processing circuit according to one of the preceding claims, wherein said zooming and up-conversion control means comprises adder means (9), line delay means (10) and line address counter means (8), wherein

said adder means receives said zoom factor as a first input and provides output data to said line delay means (10),

said line delay means (10) provides output data to said interpolation means and to said adder means as a second input thereof,

said line address counter (8) receives a MSB from the output of the line delay means and controls by its output the read-out of the first field memory.

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7. Digital signal processing circuit according to claim 5, wherein said adder means is a 7-bit adder and said line delay means provides the six lower bits of its output to the second input of the adder means and to the interpolation means and provides the most significant bit of its output to said line address counter means (8).

8. Digital signal processing circuit according to one of the claims 1-5, wherein said digital signal further comprises:

a second field memory (12), a second interpolation means (13) and a mixer means (14), wherein,

said second field memory is coupled to the output of the first field memory,

said second interpolation means (13) receives as a first input an output of the second field memory (12), as a second input the output of the first field memory (1') and as a third input a one-line-delayed version of the output of the first field memory and generates, based on either the first and second or the first and third inputs, interpolated line data,

said mixer means (14) receives the output data from the first and the second interpolation means (2', 13) and generates output data based on the two inputs and based on a motion signal supplied by a motion detection unit.

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9. Digital signal processing circuit according to claim 8, wherein said second interpolation means is an FIR-filter and preferably a 2-tap FIR-filter.

10. Digital signal processing circuit according to claim 9, wherein said FIR-filter comprises weighting means (16) which are controlled by said zooming and up-conversion means (3; 11).

11. Digital signal processing circuit according to claim 10, wherein said FIR-filter comprises multiplexer means (17, 18) for passing either the first and second or first and third input to the FIR-filter.

12. Digital signal processing circuit according to one of the claims 8-11, wherein said zooming and up-conversion means (11) controls the weighting operation performed within the first interpolation means and the weighting operation performed by the second interpolation means and further controls the switching of the multiplexer means (17, 18) contained in the second interpolation means (13).

13. Digital signal processing circuit according to one of the claims 8-12, wherein the third input to the second interpolation means is provided by a line delay means which is included in said first interpolation means.