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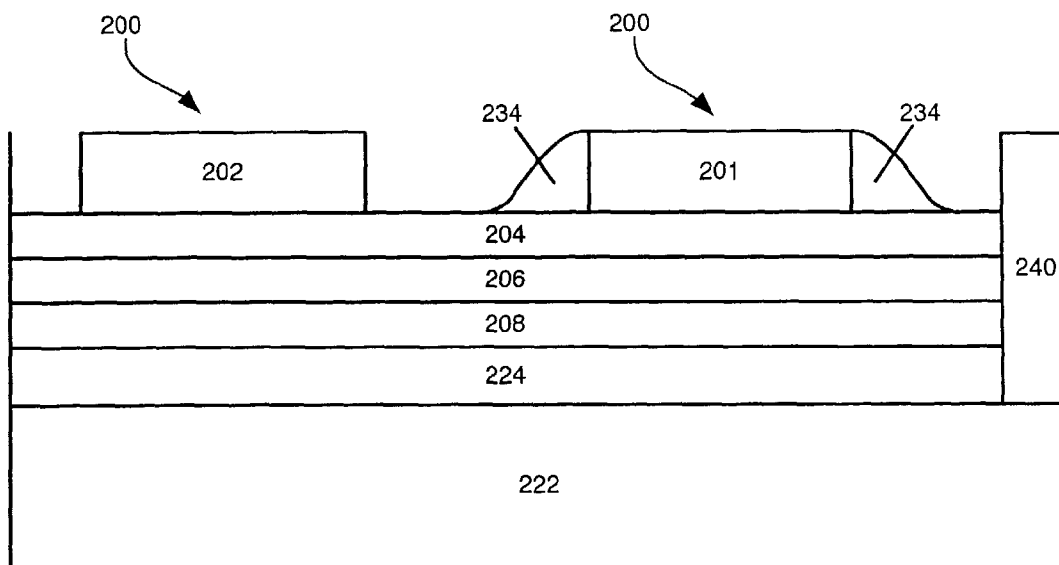
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(54) Title: CHARGE-TRAPPING MEMORY ARRAYS



(57) Abstract: The present invention relates to a memory array (100) comprising a substrate (222) and a plurality of bitlines (224) having contacts (240) and a plurality of wordlines (201, 202) intersecting the bitlines (224). A protective spacer (234) is used to separate the bitline contacts (240) from the wordlines (201) adjacent to the bitline contacts (240) to prevent damage caused during the formation of the bitline contacts (240). The present invention also relates to a method of forming the memory array.

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