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A Method For An Advanced MIM Capacitor

Abstract

A method for forming a capacitor in a semiconductor device. An embodiment simultaneously forms a MIM capacitor and a dual damascene interconnect using common process steps. An embodiment comprises: forming a capacitor bottom plate and a first metal line over the semiconductor structure. We form a second dielectric layer over the capacitor bottom plate, the first metal line, and a first dielectric layer. Next, we form a top plate opening in the second dielectric layer to at least partially expose the capacitor bottom plate. A capacitor dielectric layer is formed over the capacitor bottom plate and the second dielectric layer. A capacitor top plate is formed in the top plate opening. Subsequently, we form a via opening through at least the second dielectric layer, the capacitor dielectric layer over the first metal line to expose a portion of the first metal line. Next, we fill the via opening with a second metal layer to form a via plug. A third dielectric layer is formed over the via plug and the capacitor top plate. We form a first trench opening and a second trench opening through the third dielectric layer, the second passivation layer and the third passivation layer. The first trench opening exposes a portion of the capacitor top plate. The second trench opening exposes a portion of the via plug. Next, we form a first trench plug in first trench opening and a second trench plug is the second trench opening. The top plate, the capacitor dielectric and the bottom plate form a capacitor.

FIGURE 1A