200301833 3
18/03/03

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 February 2003 (27.02.2003)

PCT

(10) International Publication Number
WO 03/017148 A1

(51) International Patent Classification[7]: G06F 17/50

(21) International Application Number: PCT/US01/25546

(22) International Filing Date: 14 August 2001 (14.08.2001)

(25) Filing Language: English

(26) Publication Language: English

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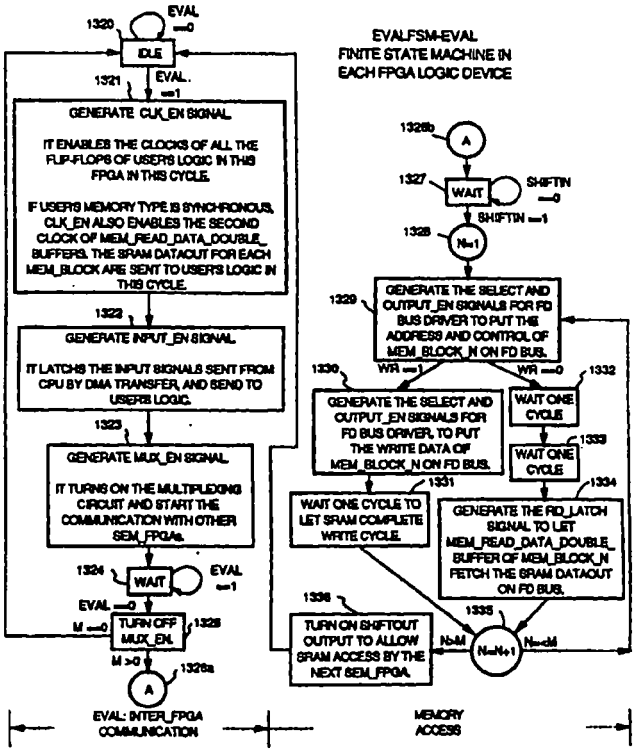
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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF,

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(54) Title: TIMING-INSENSITIVE GLITCH-FREE LOGIC SYSTEM AND METHOD



(57) Abstract: A timing insensitive glitch-free (TIGF) logic device which can take the form of any latch or edge triggered flip-flop. In one embodiment, a trigger signal is provided to update the TIGF logic device. The trigger signal is provided during a short trigger period that occurs at adjacent times from the evaluation period (figure 59). In latch form, the TIGF latch includes a flip-flop that holds the current state of the TIGF latch until a trigger signal is received (figure 59). A multiplexer is also provided to receive the new input value and the old stored value. The enable signal functions as the selector signal for the multiplexer. In flip-flop form, the TIGF flip-flop includes a first flip-flop that holds the new input value, a second flip-flop that holds the current stored value, and a clock edge detector. Hold time violations are avoided because one dedicated flip-flop stores the new input value which effectively blocks input changes during evaluation.

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CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

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