**A METHOD TO FORM A VERTICAL TRANSISTOR BY SELECTIVE EPITAXIAL GROWTH AND DELTA DOPED SILICON LAYERS**


## Abstract

A method for a vertical transistor by selective epi deposition to form the conductive source, drain, and channel layers. The conductive source, drain, and channel layers are preferably formed by a selective epi process. Dielectric masks define the conductive layers and make areas to form vertical contacts to the conductive S/D and channel layers.


Fig. 7