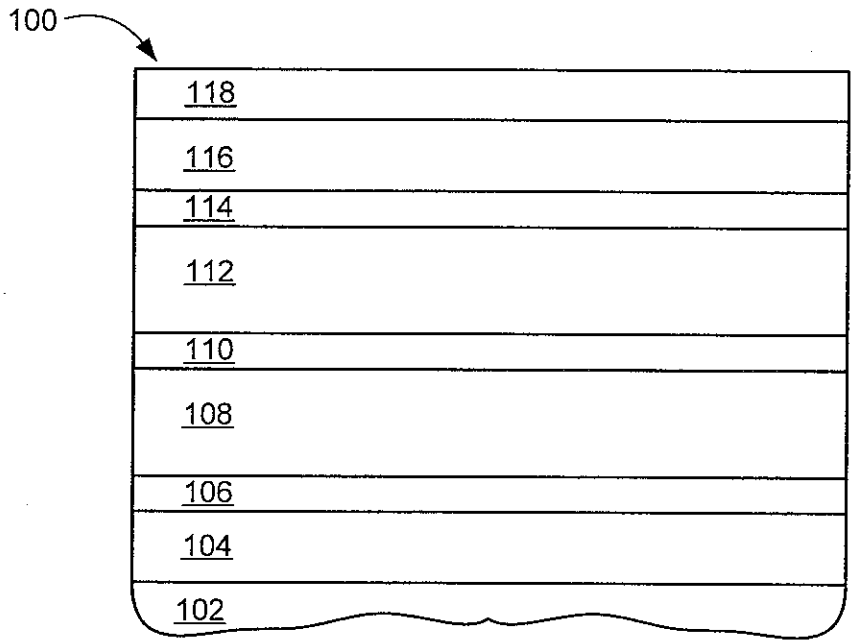

100
118
116
114
112
110
108
106
104
102

FIG. 1

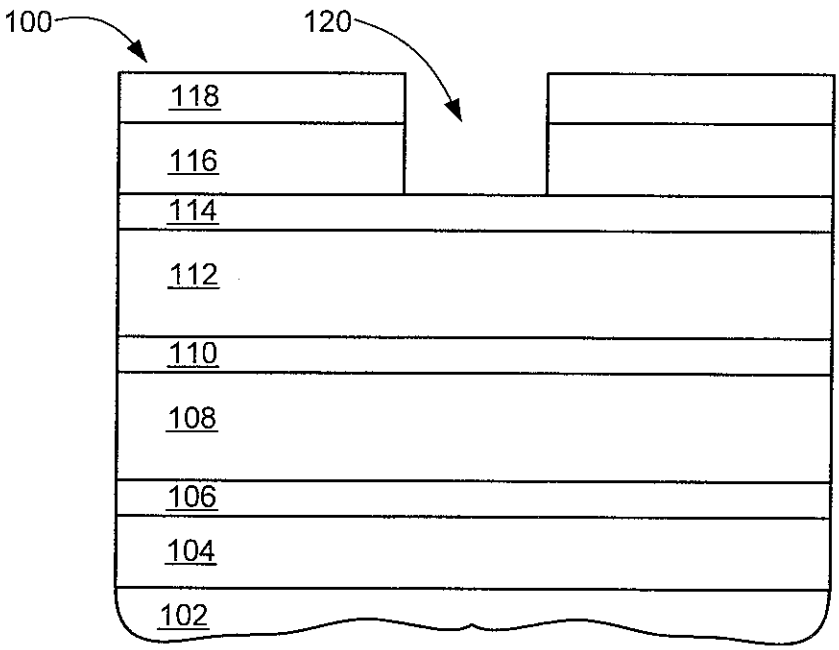

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FIG. 2

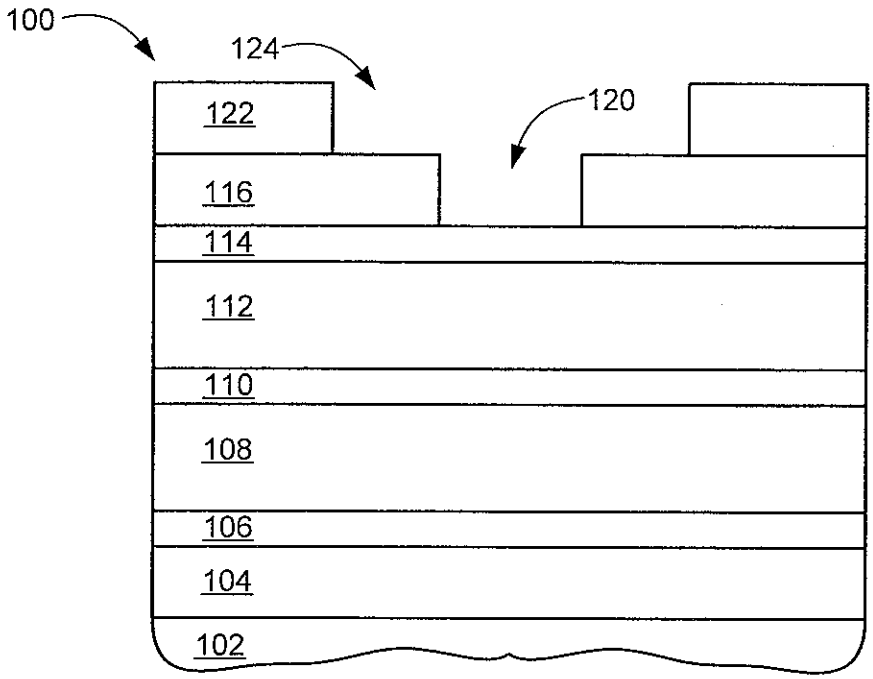

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122
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FIG. 3

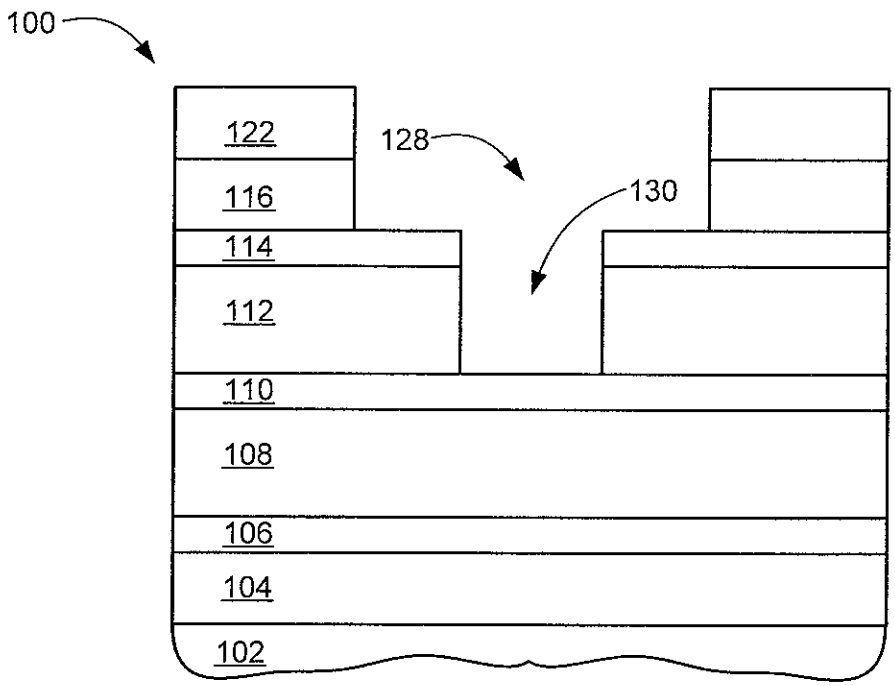

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122
128
130
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102

FIG. 4

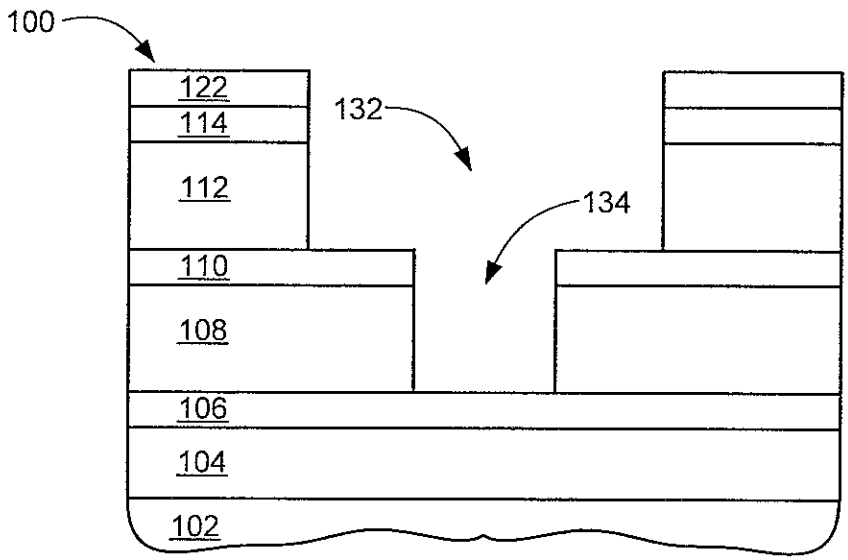

100
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102

FIG. 5

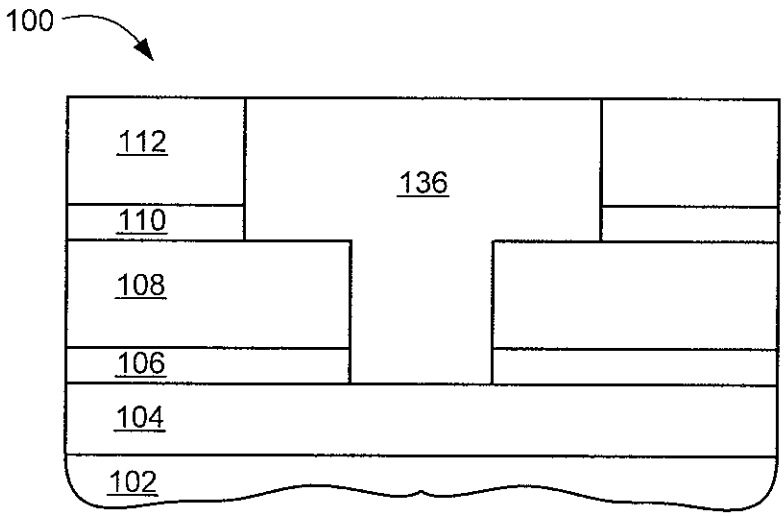

100
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104
102

FIG. 6

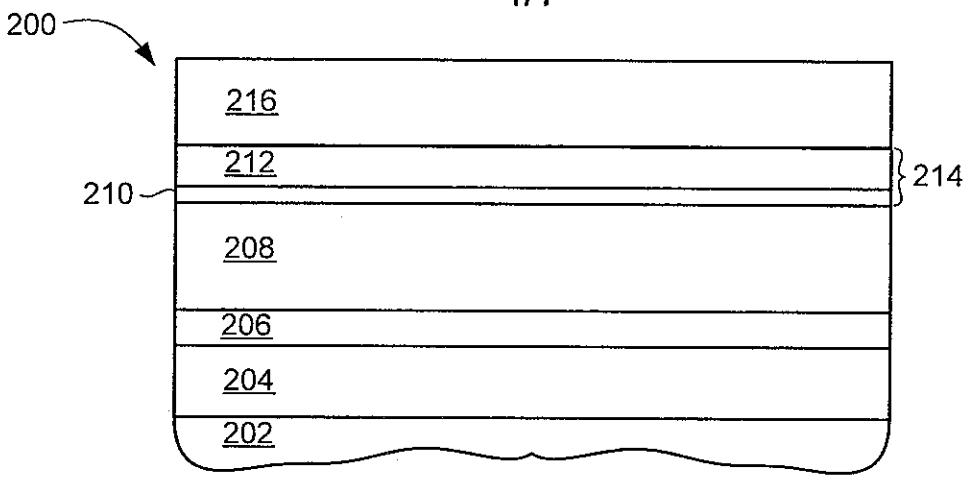


FIG. 7

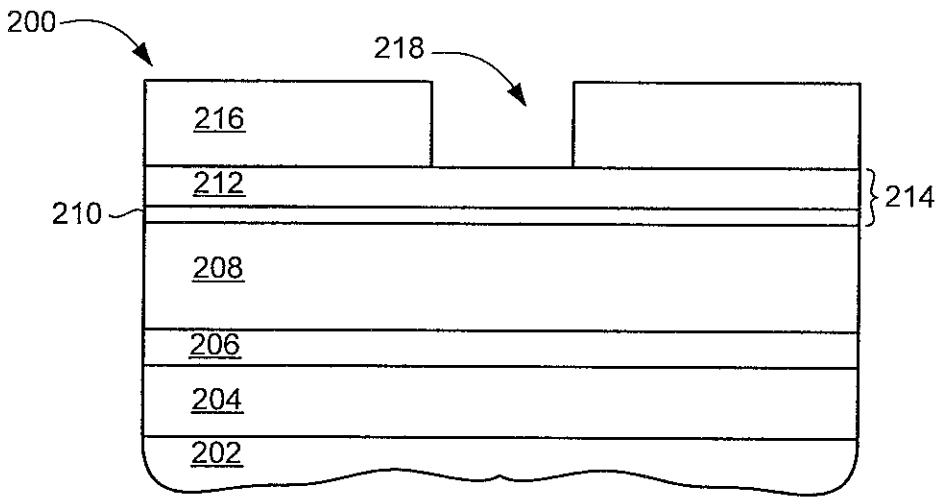


FIG. 8

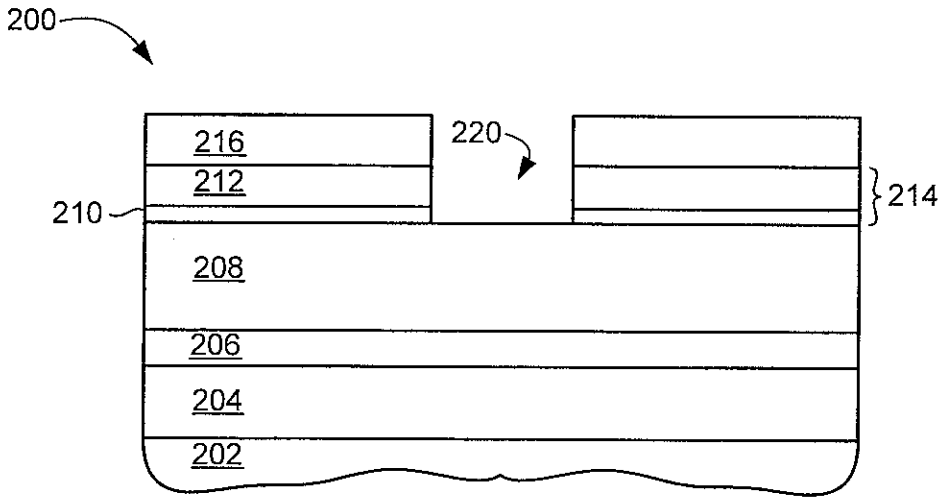


FIG. 9

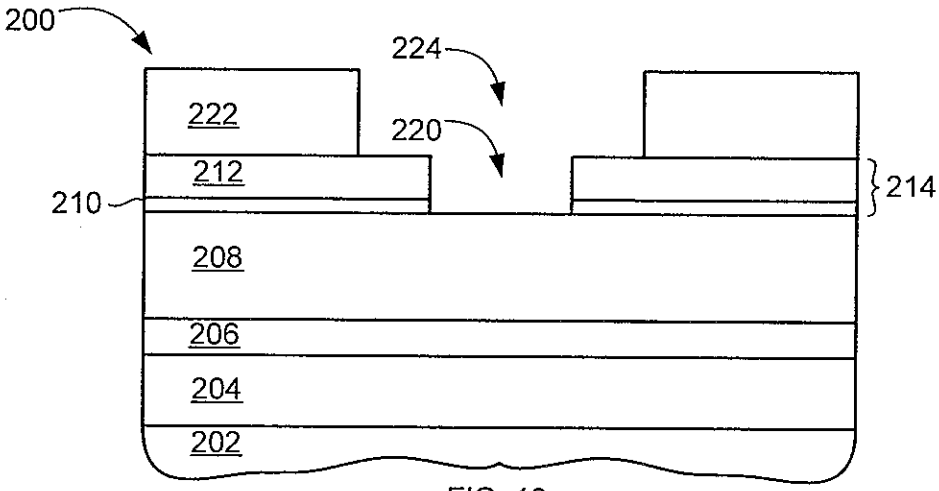


FIG. 10

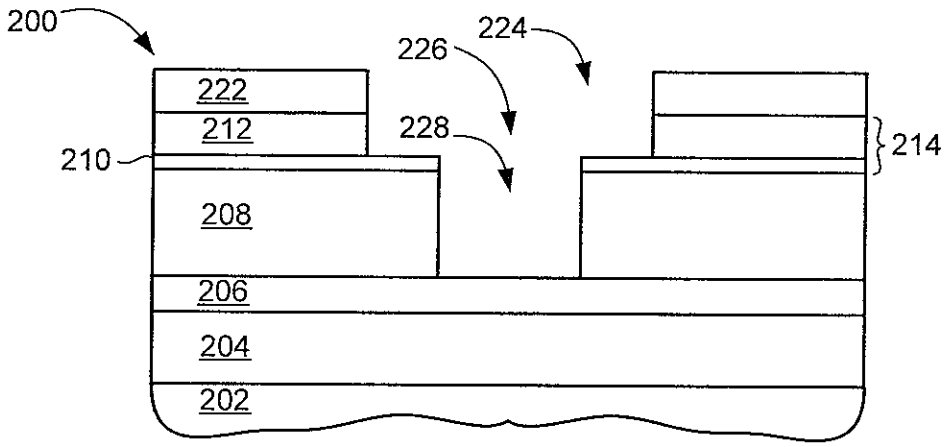


FIG. 11

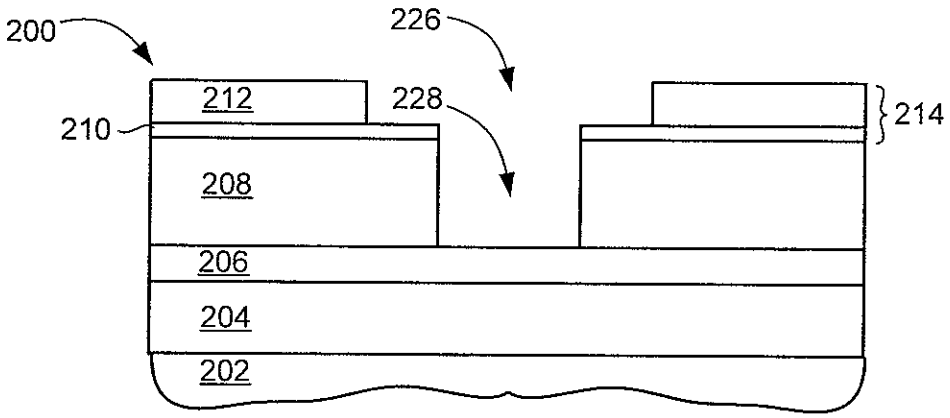


FIG. 12

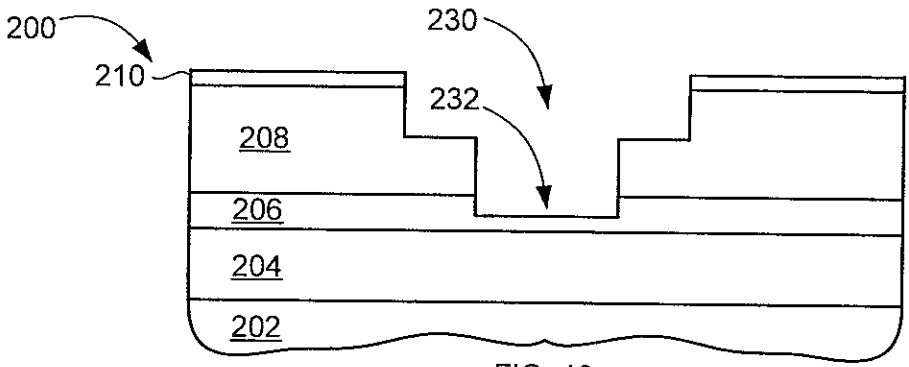


FIG. 13

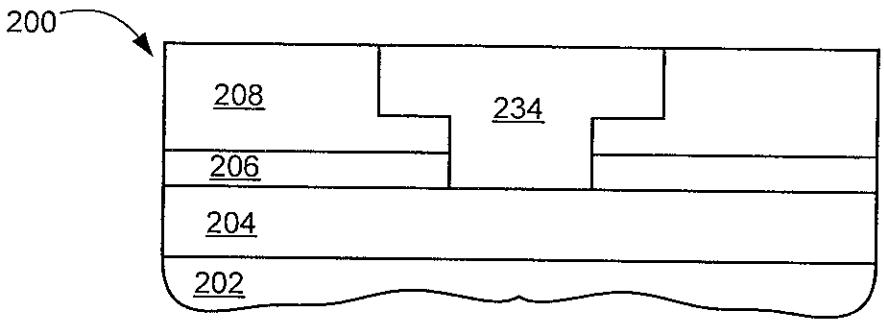


FIG. 14

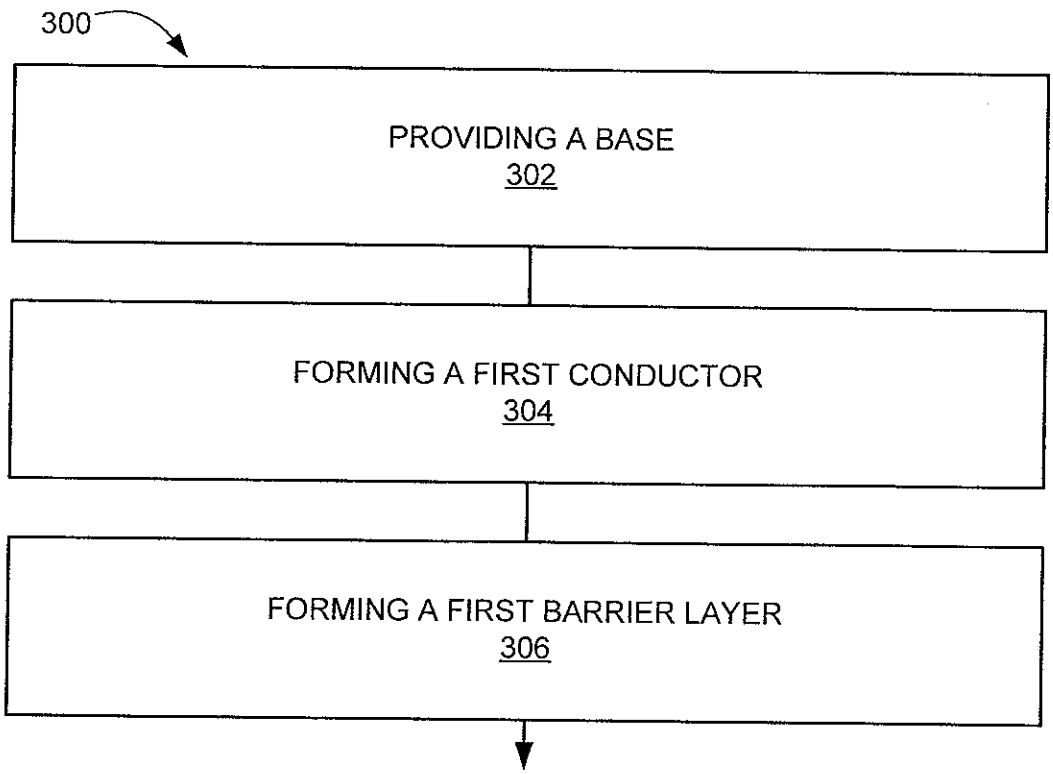


FIG. 15A

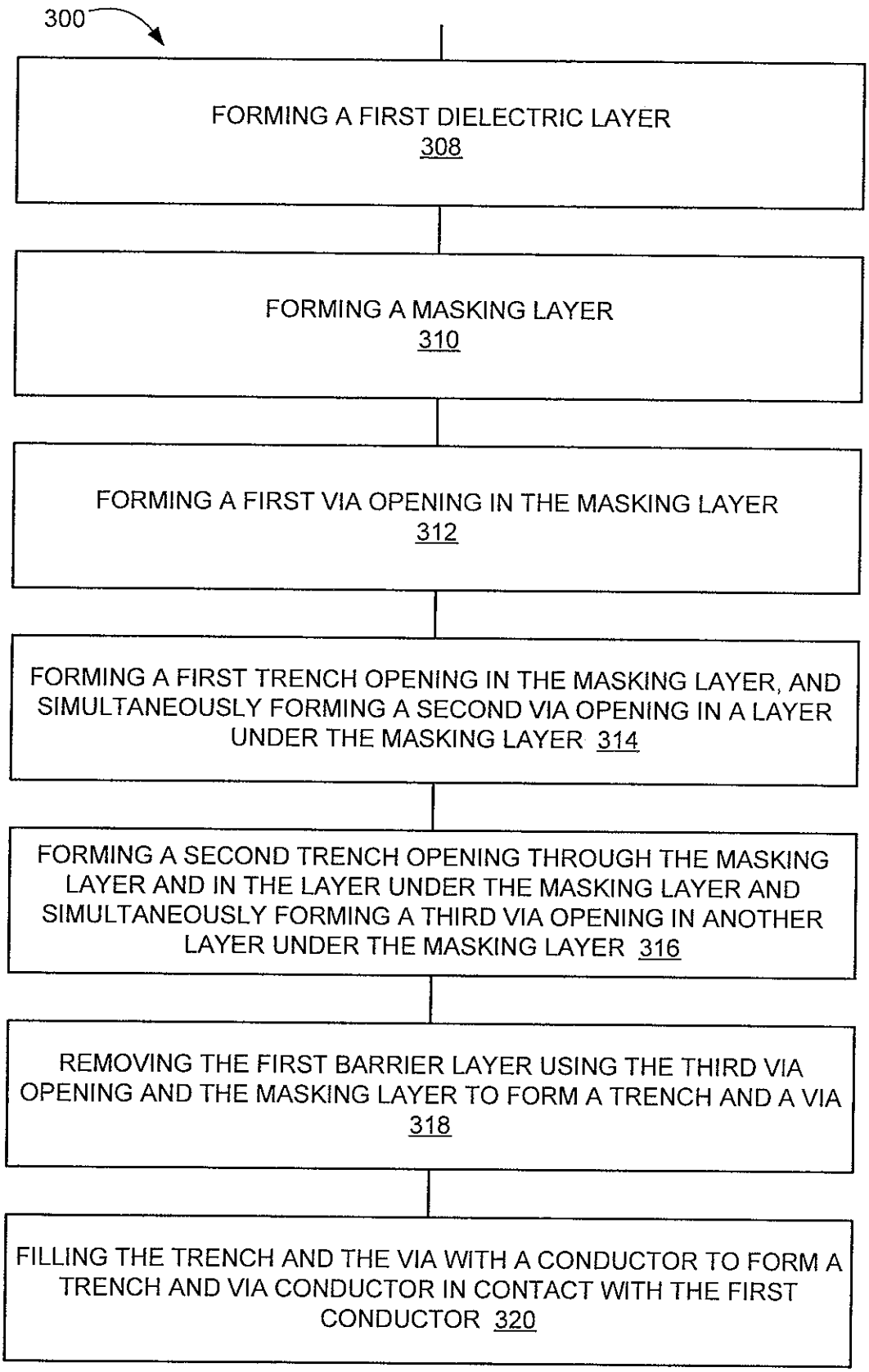

300
FORMING A FIRST DIELECTRIC LAYER 308
FORMING A MASKING LAYER 310
FORMING A FIRST VIA OPENING IN THE MASKING LAYER 312
FORMING A FIRST TRENCH OPENING IN THE MASKING LAYER, AND SIMULTANEOUSLY FORMING A SECOND VIA OPENING IN A LAYER UNDER THE MASKING LAYER 314
FORMING A SECOND TRENCH OPENING THROUGH THE MASKING LAYER AND IN THE LAYER UNDER THE MASKING LAYER AND SIMULTANEOUSLY FORMING A THIRD VIA OPENING IN ANOTHER LAYER UNDER THE MASKING LAYER 316
REMOVING THE FIRST BARRIER LAYER USING THE THIRD VIA OPENING AND THE MASKING LAYER TO FORM A TRENCH AND A VIA 318
FILLING THE TRENCH AND THE VIA WITH A CONDUCTOR TO FORM A TRENCH AND VIA CONDUCTOR IN CONTACT WITH THE FIRST CONDUCTOR 320

FIG. 15B