

CLAIMS

1. A computer program product for executing a machine instruction in a central processing unit, the computer program product comprising:

a computer readable storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method comprising:

obtaining, by a processor, a machine instruction for execution, the machine instruction being defined for computer execution according to a computer architecture, the machine instruction comprising:

at least one opcode field to provide an opcode, the opcode identifying a Vector Checksum operation;

a first register field to be used to designate a first register, the first register comprising a first operand;

a second register field to be used to designate a second register, the second register comprising a second operand; and

an extension field to be used in designating one or more registers, and wherein the first register field is combined with a first portion of the extension field to designate the first register, the second register field is combined with a second portion of the extension field to designate the second register; and

executing the machine instruction, the executing comprising:

adding together a plurality of elements of the second operand to obtain a first result, wherein the adding comprises performing one or more end around carry add operations;

based on performing an end around carry add operation and producing a sum, adding a carry out of a chosen position of the sum, if any, to a selected position in a selected element of the first operand; and

placing the first result in the selected element of the first operand.

2. The computer program product of claim 1, wherein the chosen position is bit position zero, the selected position is bit position 31, and the selected element of the first operand is element one of the first operand.

3. The computer program product of claim 2, wherein the executing further comprises placing zeros in one or more other elements of the first operand.

4. The computer program product of claim 3, wherein the first operand comprises four word-sized elements, and wherein the placing comprises placing zeros in elements zero, two and three of the first operand.
5. The computer program product of claim 1, wherein the plurality of elements of the second operand comprises a plurality of word-sized elements.
6. The computer program product of claim 1, wherein the machine instruction further comprises a third register field to be used to designate a third register, the third register comprising a third operand, and wherein the executing further comprises adding the first result to a selected element of the third operand to obtain a second result, the adding the first result using an end around carry add operation.
7. The computer program product of claim 1, wherein the executing further comprises adding the first result to a selected element of a third operand to obtain a second result, the adding the first result using an end around carry add operation, and wherein the placing comprises placing the second result in the selected element of the first operand.
8. The computer program product of claim 7, wherein the third operand is included in the machine instruction.
9. A computer system for executing a machine instruction in a central processing unit, the computer system comprising:
 - a memory; and
 - a processor in communications with the memory, wherein the computer system is configured to perform a method, said method comprising:
 - obtaining, by a processor, a machine instruction for execution, the machine instruction being defined for computer execution according to a computer architecture, the machine instruction comprising:
 - at least one opcode field to provide an opcode, the opcode identifying a Vector Checksum operation;
 - a first register field to be used to designate a first register, the first register comprising a first operand;
 - a second register field to be used to designate a second register, the second register comprising a second operand; and

an extension field to be used in designating one or more registers, and wherein the first register field is combined with a first portion of the extension field to designate the first register, the second register field is combined with a second portion of the extension field to designate the second register; and

executing the machine instruction, the executing comprising:

adding together a plurality of elements of the second operand to obtain a first result, wherein the adding comprises performing one or more end around carry add operations;

based on performing an end around carry add operation and producing a sum, adding a carry out of a chosen position of the sum, if any, to a selected position in a selected element of the first operand; and

placing the first result in the selected element of the first operand.

10. The computer system of claim 9, wherein the chosen position is bit position zero, the selected position is bit position 31, and the selected element of the first operand is element one of the first operand.

11. The computer system of claim 9, wherein the plurality of elements of the second operand comprises a plurality of word-sized elements.

12. The computer system of claim 9, wherein the machine instruction further comprises a third register field to be used to designate a third register, the third register comprising a third operand, and wherein the executing further comprises adding the first result to a selected element of the third operand to obtain a second result, the adding the first result using an end around carry add operation.

13. The computer system of claim 9, wherein the executing further comprises adding the first result to a selected element of a third operand to obtain a second result, the adding the first result using an end around carry add operation, and wherein the placing comprises placing the second result in the selected element of the first operand.

14. The computer system of claim 13, wherein the third operand is included in the machine instruction.

15. A method of executing a machine instruction in a central processing unit, the method comprising:

obtaining, by a processor, a machine instruction for execution, the machine instruction being defined for computer execution according to a computer architecture, the machine instruction comprising:

at least one opcode field to provide an opcode, the opcode identifying a Vector Checksum operation;

a first register field to be used to designate a first register, the first register comprising a first operand;

a second register field to be used to designate a second register, the second register comprising a second operand; and

an extension field to be used in designating one or more registers, and wherein the first register field is combined with a first portion of the extension field to designate the first register, the second register field is combined with a second portion of the extension field to designate the second register; and

executing the machine instruction, the executing comprising:

adding together a plurality of elements of the second operand to obtain a first result, wherein the adding comprises performing one or more end around carry add operations;

based on performing an end around carry add operation and producing a sum, adding a carry out of a chosen position of the sum, if any, to a selected position in a selected element of the first operand; and

placing the first result in the selected element of the first operand.

16. The method of claim 15, wherein the chosen position is bit position zero, the selected position is bit position 31, and the selected element of the first operand is element one of the first operand.

17. The method of claim 16, wherein the executing further comprises placing zeros in one or more other elements of the first operand.

18. The method of claim 17, wherein the first operand comprises four word-sized elements, and wherein the placing comprises placing zeros in elements zero, two and three of the first operand.

19. The method of claim 15, wherein the plurality of elements of the second operand comprises a plurality of word-sized elements.

20. The method of claim 15, wherein the machine instruction further comprises a third register field to be used to designate a third register, the third register comprising a third operand, and wherein the executing further comprises adding the first result to a selected element of the third operand to obtain a second result, the adding the first result using an end around carry add operation.

21. The method of claim 15, wherein the executing further comprises adding the first result to a selected element of a third operand to obtain a second result, the adding the first result using an end around carry add operation, and wherein the placing comprises placing the second result in the selected element of the first operand.

22. The method of claim 21, wherein the third operand is included in the machine instruction.