2003011640

11 MAR 2003

162162

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 March 2002 (28.03.2002)

PCT

(10) International Publication Number
WO 02/25700 A3

(51) International Patent Classification[7]: H01L 29/06, 29/739, 29/78, 27/088

(21) International Application Number: PCT/GB01/04211

(22) International Filing Date:
20 September 2001 (20.09.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/234,219 21 September 2000 (21.09.2000) US

(71) Applicant: CAMBRIDGE SEMICONDUCTOR LIMITED [GB/GB]; University Challenge Fund, 16 Mill Lane, Cambridge CB2 1SB (GB).

(72) Inventors: UDREA, Florin; 95 Burnside, Cambridge CB1 3PA (GB). AMARATUNGA, Gehan, Anil, Joseph; 235 Hills Road, Cambridge CB2 2RW (GB).

(74) Agent: FLINT, Adam; W.H. Beck, Greener & Co., 7 Stone Buildings, Lincoln's Inn, London WC2A 3SZ (GB).

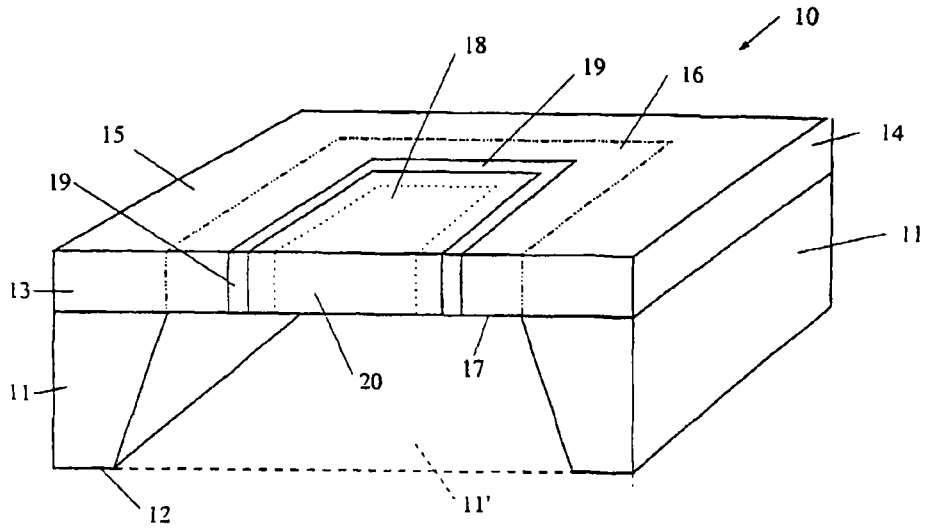
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) Title: SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SEMICONDUCTOR DEVICE



(57) Abstract: A power semiconductor device (10) has an active region that includes a drift region (20). At least a portion of the drift region (20) is provided in a membrane)16) which has opposed top and bottom surfaces (15, 17). In one embodiment, the top surface (15) of the membrane (16) has electrical terminals connected directly or indirectly thereto to allow a voltage to be applied laterally across the drift region (20). In another embodiment, at least one electrical terminal is connected directly or indirectly to the top surface (15) and at least one electrical terminal is connected directly or indirectly to the bottom surface (17) to allow a voltage to be applied vertically across the drift region (20). In each of these embodiments, the bottom surface (17) of the membrane (16) does not have a semiconductor substrate positioned adjacent thereto.

WO 02/25700 A3

ACTION